SYOE 4: Organic Transistors

Time: Tuesday 9:30–11:15 Location: H1

Invited Talk SYOE 4.1 Tue 9:30 H1

Vapor and Solution Deposited Small Molecule Organic Thin Film Transistors — •Thomas Jackson — Center for Thin Film Devices and Materials Research Institute, Department of Electrical Engineering, Penn State University, University Park, PA, USA, 16802

Organic thin film transistor (OTFT) device performance rivals or exceeds that of a-Si:H devices, and low OTFT processing temperature allows fabrication on a variety of surfaces including cloth, paper, or polymeric substrates. For device and system use, OTFTs must demonstrate the uniformity, reproducibility, reliability, and integration with other devices needed for practical applications. As an application demonstration we have integrated vapor-deposited OTFTs with organic light emitting diodes (OLEDs) and have fabricated small test displays on polyester substrates to investigate device characteristics and passivation and isolation requirements.

Many organic device applications are likely to be cost sensitive and solution-deposited organic semiconductors offer important advantages for low-cost processing. However, solution processed semiconductors typically lack the molecular-level order which may be necessary for good carrier transport and large field-effect transistor mobility. Working with J. Anthony (University of Kentucky) we have investigated functionalized pentacenes and pentacene derivatives. Surprisingly, solution-deposited films of some of these materials show good molecular ordering and, using these materials, we have fabricated simple circuits, including ring oscillators, and OTFTs with mobility $>$ 2 cmˆ2/V-s.

SYOE 4.2 Tue 10:15 H1

Dielectric Interface Modification by UV irradiation: A Novel Method to control OFET charge carrier transport properties — •Niels Benson, Martin Schidleja, Christian Melzer, and Heinz von Seggern — University of Technology Darmstadt, Institute of Material Science, Petersenstr. 23, 64287 Darmstadt, Germany

In the present talk a novel concept is introduced, which allows for a change in OFET polarity by polymer dielectric interface modification. This concept is based on the irradiation of the gate dielectric by ultra violet radiation prior to the organic semiconductor deposition. As a result balanced unipolar charge carrier transport properties of n- and p-type pentacene based OFETs were obtained. The change in OFET polarity manifests itself in a large positive threshold voltage shift of approximately 60V for both charge carrier types. On the basis of detailed studies using contact angle and x-ray photo electron spectroscopy measurements, a possible cause for the threshold voltage shift is discussed. We could show that during the UV treatment step, polar groups such as C=O and according to literature -COH, recently identified as electron traps by Chua et al., are formed in the polymeric gate dielectric, influencing the OFET charge carrier properties. In line with this idea, negative charge carriers are localized within the PMMA dielectric once the UV modified OFET is driven in electron accumulation mode. This results in a positive threshold voltage shift inhibiting the electron- and promoting the hole-transport. The area density of trapped electrons necessary for the observed threshold voltage shift is estimated to be $\geq 3.9{*}10^{12}\mathrm{cm}^{-2}$.

SYOE 4.3 Tue 10:30 H1

Electric field induced gap states in pentacene — •Dietmar Knipp[1], Amare Benor[1], Arne Hoppe[1], Veit Wagner[1], and Armin Völkel[2] — [1]International University Bremen, School of Engineering and Science , 28759 Bremen, Germany — [2]Palo Alto Research Center, Electronic Materials and Device Laboratory, Palo Alto, California, USA

Despite the realization of pentacene transistors with high mobility the electronic transport is not fully understood. In particular the creation of gap states and the influence of gap states on the charge transport are still under investigation. To study the creation of electronic defects electrical in-situ measurements of pentacene TFTs were carried out. The devices with hole mobilities ranging from 0.2-0.5cm^2/Vs were exposed to oxygen and moisture to study the influence on the device characteristic. Exposing the transistor to oxygen does not lead to a change of the transistor characteristic. Only if an electric field is applied while exposing the devices to oxygen a change of the device characteristic is observed. Applying voltages to the device leads to a shift of the onset of the drain current towards positive gate voltages. As a consequence the subthreshold slope is destinclty increased. The threshold voltage and the mobility are not affected by the oxygen contamination. Numerical simulations of the device charateristic reveal that the onset of the drain current is caused by acceptor-like defect states deep in the bandgap. A good agreement between the simulation and the experiment was observed by using a Gaussian distribution of defect states.

SYOE 4.4 Tue 10:45 H1

Spatially-Resolved Photoresponse Measurements on Pentacene Thin-Film Transistors — Matthias Fiebig[1], Christoph Erlen[2], Paolo Lugli[2], Udo Beierlein[1], and •Bert Nickel[1] — [1]Dep. für Physik und CeNS, Ludwig-Maximilians-Universität, München — [2]Institute for Nanoelectronics, Technische Universität München

Spatially resolved photoresponse has been measured on pentacene thin film transistors. The technique allows for the investigation of the response to illumination with a spatial resolution in the submicron regime. Enhanced photoresponse was observed close to the negatively biased electrode. We have modelled the experiment using drift-diffusion simulations and a photo doping mechanism. In this model holes in pentaene can drift, while electrons remain almost fixed at their site of generation until they recombine. The electron lifetime extracted from this model is in the order of 10 ps.

SYOE 4.5 Tue 11:00 H1

Reduced contact and sheet resistance in bottom-contact pentacene field-effect transistors using palladium electrodes — •D. V. Pham[1], G. Deck[1], C. Bock[1], U. Kunze[1], D. Käfer[2], G. Witte[2], and Ch. Wöll[2] — [1]Lehrstuhl für Werkstoffe und und Nanoelektronik, Ruhr-Universität Bochum, D-44780 — [2]Lehrstuhl für Physikalische Chemie I, Ruhr-Universität Bochum, D-44780

The influence of the source and drain contact metals (Au, Pd, and Pt) on the morphology and on the OFET performance was investigated. The devices consisted of metal source and drain electrodes contacting a 110-nm-thick pentacene film thermally deposited on SiO_2 dielectrics (d = 40 nm) with an n^+-doped Si substrate serving as the gate electrode. Transistors with channel lengths from $L = 3$ μm to 100 μm at a constant channel width $w = 2$ mm are prepared in order to separate the sheet resistance from the parasitic resistance of the contacts and leads. The contact resistance of transistors with Pd electrodes is four times smaller and the sheet resistance is eight times smaller than those of transistors with Pt or Au electrodes. The reduced sheet resistance is also reflected by a reduced trap density. Although Pt has a higher work function than Au and Pd the transistors with Au and Pt electrodes have similarly electrical characteristics. This can be explained by the film morphology. In order to study the nucleation of the pentacene on the OFET substrate further samples are prepared with an 8-nm-thick pentacene film. While the growth on the Au and Pt electrodes is completely different to the film morphology on silicon dioxide the growth on Pd is smiliarly to that on the insulator.