T 23: DAQ, Trigger, Elektronik 1

Zeit: Montag 11:00–12:30 Raum: GFH 01-731

T 23.1 Mo 11:00 GFH 01-731

Performance and test results of the new IBL read-out system — •Marcello Bindi[1], Arnulf Quadt[1], Jörn Grosse-Knetter[1], Andreas Kugel[2], and Tobias Flick[3] — [1]Georg-August-University of Göttingen, II. Physikalisches Institut Friedrich-Hund-Platz 1, 37077 Goettingen, Germany — [2]Universität Heidelberg — [3]Bergische Universität Wuppertal

The upgrade for the ATLAS detector will undergo different phases towards HL-LHC. The first upgrade for the Pixel Detector will consist of the construction of a new pixel layer which will be installed during the long shutdown of the LHC machine in 2013/14 (Phase 0 Upgrade). The new detector, called Insertable B-Layer (IBL), will be inserted between the existing pixel detector and a new beam-pipe at a (smaller) radius of about 3.2 cm. The IBL requires the development of several new technologies to cope with the increase of radiation and pixel occupancy as well as to improve the physics performance of the existing pixel detector. 12 million pixels attached to new FE-I4 readout ASICs will require new off-detector electronics which is currently realized with two VME-based boards: a Back Of Crate module implementing optical I/O functionality and a Readout Driver module for data processing. An overview of the new IBL read-out system will be presented, focusing on the integration work performed at CERN with the production components. In order to finalize strategies for the system commissioning, data taking and calibration tests have been run. The outcome of these tests will also be discussed.

T 23.2 Mo 11:15 GFH 01-731

The Data Handling Processor of the Belle II DEPFET Detector — •Leonard Germic, Tomasz Hemperek, Tetsuichi Kishishita, Hans Krüger, Mikhail Lemarenko, Florian Lütticke, Carlos Marinas, and Norbert Wermes — Physikalisches Institut, Universitaet Bonn, Deutschland

A two layer highly granular DEPFET pixel detector will be operated as the innermost subsystem of the Belle II experiment, at the new Japanese super flavor factory (SuperKEKB). Such a finely segmented system will allow to improve the vertex reconstruction in such ultra high luminosity environment but, at the same time, the raw data stream generated by the 8 million pixel detector will exceed the capability of real-time processing due to its high rate. For this reason a new ASIC, the Data Handling Processor (DHP) is designed to provide full functionality of zero-suppression, data reduction and data transmission at the level of the front-end electronics. In this contribution, the description of the latest prototype chip in TSMC 65 nm technology together with the latest test results including the data processing quality and the signal integrity of the gigabit transmission lines will be presented.

T 23.3 Mo 11:30 GFH 01-731

STiC v2 - A Silicon Photomultiplier Readout ASIC with Very High Timing Resolution — •Huangshan Chen — Kirchhoff Institut fur Physik, Universitat Heidelberg

STiC v2 is a 16-channel mixed mode readout ASIC for Silicon Photomultiplier (SiPM) with very high timing resolution. The chip is designed in UMC 0.18um COMS technology and aiming for ToF applications in medical imaging and High Energy Physics (HEP). The differential frontend of the chip is designed to reject the common-mode noise from both internal digital parts and external sources. However, the chip allows for either single-ended connection or differential connection to SiPM. The time and charge information from the SiPM signals are encrypted into two time stamps, which are then processed by the build-in TDC module with a time resolution better than 20ps. The digitized data is first stored in an on-chip memory and then transferred to external DAQ system over a 160Mbit/s LVDS serial link using 8/10bit encoding. The chip provides a linear SiPM bias tuning range of ~700mV to compensate the breakdown voltage variation of SiPMs. A special linearized time over threshold technique has been implemented to provide a linear response to the charges from 3pC to several nC. A Single Photon Time Resolution (SPTR) of ~180ps has been measured with a fast laser system and Hamamatsu MPPC S10362-11-100. With Hamamatsu MPPC S10362-33-050C, 3.1mmx3.1mmx15mm LYSO crystals and 22Na source, a minimum Coincidence Time resolution (CTR) of ~220ps has been obtained using STiC v2. Future applications in HEP are the tile and fiber trackers for the planned Mu3e experiment.

T 23.4 Mo 11:45 GFH 01-731

ASIC-Based Readout for a Large-Scale COBRA Experiment — •Oliver Schulz — Max-Planck-Institut f. Physik, München

The COBRA-experiment searches for neutrinoless double beta decays, especially of ^{116}Cd, using CdZnTe semiconductor detectors.

Currently, the COBRA underground setup employs discrete amplifiers and rack-based digitizers to read out the signals of the detector crystals. For the large-scale experiment ultimately envisioned, however, such a readout may not be feasible.

An integrated solution would make it possible to move the complete readout, including digitization, near the detectors. It would severely reduce the amount of cabling required within the ultra-low background region of the experiment, in comparison to external electronics. It would also come at lower cost and power consumption and require significantly less space.

We present the results of first tests using an ASIC, with integrated charge amplifiers and switched-capacitor array sampling, to directly read out coplanar-grid (CPG) CdZnTe detector signals, including pulse shape recording.

T 23.5 Mo 12:00 GFH 01-731

Parallelisierte Auslese von FE-I4 Vierchipmodulen mit USBpix — •Johannes Agricola, Jörn Grosse-Knetter und Arnulf Quadt — II. Physikalisches Institut, Georg-August-Universität Göttingen

Die Existenz kosteneffizienter Detektorauslesesysteme für Prototypen und kleine Aufbauten ist elementar für die verteilte Entwicklung moderner Detektoren. USBpix, das auf USB basierende Einzelmodulauslesesystem für ATLAS-Pixeldetektoren, wurde bereits intensiv im Rahmen des Insertable B-Layer (IBL) für Test und Fertigung verwendet. Die geplanten Neuerungen am Pixel-System des ATLAS-Experiments wie Module mit mehr als zwei Chips und Multiplexverfahren auf den Daten- und Steuerleitungen erfordern grundlegende Anpassungen in dessen Software. Die Ergebnisse aus der Evaluation einer neuen FPGA-Konfiguration für USBpix, welche die parallelisierte Auslese von Modulen mit vier FE-I4 Auslesechips, wird vorgestellt und die Machbarkeit diverser Maßnahmen zur Reduktion der Zahl elektrischer Kommunikationskanäle gezeigt.

T 23.6 Mo 12:15 GFH 01-731

STiC3 - A chip for pico-seconds Time-of-Flight Applications — •Vera Koleva Stankova, Tobias Harion, and Wei Shen — Kirchhoff-Institute for Physics, Im Neuenheimer Feld, 227 D-69120 Heidelberg

STiC is a recently developed application specific integrated circuit (ASIC) for time-of-flight measurements in high energy physics and medical imaging applications. It is a 64-channel mixed mode ASIC designed in the UMC 0.18 μm CMOS technology for the readout of silicon photomultipliers (SiPM), dedicated to the ENDOToFPET-US project. The project aims at the development of a precise endoscopic PET probe for early pancreas and prostate cancer detection with a spatial resolution of 1 mm and a time-of flight resolution of 200 ps. The 64-channel chip has a size of only 5x5 mm^2 and each channel consist of an analog and a digital part. The analog front-end part provides the information of the input signal in terms of a shaped pulse which is proportional to the input charge. The digital part integrates a time-to digital converter (TDC) with a timing resolution of 20 ps which generates two times stamps from the analog pulse. The TDC data is stored into a FIFO memory. Later the data is encoded (8/10Bit) and send to a pc with 160 MBit/s serial link. The nominal power is estimated to 25 mW per channel. The detail for the chip design and first measurements result with a SiPM and a LYSO scintillator crystal will be presented.