DS 40: Focussed Session: Memristive Devices for Neuronal Systems II

Today's computer science is characterized by a time of upheaval. The extremely successful down scaling of CMOS devices and circuit integration during the last decades will soon face physical limits. The predictable fade away of Moore-law, puts advance device structures paired with conceptual new non-Boolean architectures, such as cellular automata, quantum computer or neuromorphic circuits, more and more into the spot light of research and industry. In this respect the symposium will focus on novel opportunities of memristive devices in the field of bio-inspired computing. This symposium aims to overview of the interdisciplinary, covering interfacial physics, and electronic properties and the theory of memristive devices up to the complex architecture in biological nerve systems. This symposium aims to provide an overview of the status quo of memristive devices in neural systems by some of the leading experts in the field. Moreover, all speakers will discuss and work out the most promising and most exciting future directions, such as cognitive computing and memristive brain chips.

Organizers: Hermann Kohlstedt (CAU Kiel), Ronald Tetzlaff (TU Dresden), and Thomas Mikolajick (TU Dresden)

Time: Thursday 15:00–16:45 Location: CHE 89

Topical Talk DS 40.1 Thu 15:00 CHE 89

Brain-inspired neurocomputing with memristive synapses — •Daniele Ielmini — Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Italy

As Moore's law of CMOS downscaling slows down, research on alternative computing devices and architectures receives an increasing interest. Among these, memcomputing and neurocomputing combine a relatively simple concept (e.g., analog/digital circuits, CMOS compatible materials, room operation operation) with attractive functionalities, such as reconfigurability, ultra-low power operation, and brain-like computing capabilities including learning and inference. Merging memcomputing and neurocomputing may result in novel conceptual schemes with high energy efficiency, high speed, excellent scalability, and brain-like computing capabilities.

This talk will show recent advances on neuro-computing using memristive synapses made of resistive switching memory (RRAM) devices. Hybrid CMOS/memristive synapses capable of spike-timing dependent plasticity (STDP) and spike-rate dependent plasticity (SRDP) will be experimentally demonstrated. Pattern learning will be demonstrated by a feedforward neural network with up to 4x4 input images, 2 post-synaptic firing neurons, handling both static and dynamic moving images. The prospects of such new achievements for brain-inspired computing will be discussed.

Topical Talk DS 40.2 Thu 15:30 CHE 89

Exploring evolutionary biology and neuromorphic computing with quantum materials — •Shriram Ramanathan — Purdue University, USA

I will introduce frontier problems in evolutionary biology, their dynamics and intimate connection to neuromorphic information processing in my presentation. I will particularly emphasize the promise of adaptive quantum materials, such as strongly correlated oxide semiconductors and contrast their physics with filamentary switches and chalcogenides. The following problems will be considered: (1) structural symmetry breaking and electronic transitions driven by external stimuli in correlated electron systems, (2) the use of electrolyte membranes to create soft interfaces for neural computing circuits and (3) disorder and extreme carrier doping to create emergent phases whose volatility can be controlled by design. Connections to artificial intelligence and synergies with circuits research that is typically materials agnostic will be highlighted.

DS 40.3 Thu 16:00 CHE 89

Implementation of memristive devices in a crossbar-based pattern recognition scheme — •Mirko Hansen, Martin Ziegler, Finn Zahari, and Hermann Kohlstedt — AG Nanoelektronik, Christian-Albrechts-Universität zu Kiel, Germany

While several neuron-based learning concepts like Hebbian learning or spike-timing-dependent-plasticity have been successfully shown using single devices, their realization of whole systems using memristive devices remains challenging. Due to the progress in the field and the increase of devices per circuit, additional problems in terms of reliability and requirements in device quality arise.

We will present simulation results for a pattern recognition scheme using the MNIST benchmark dataset[1]. Parameters for these simulations were extracted from automated pulse measurements on niobium-oxide based double barrier memristive devices (Nb/Al-AlO_x/Nb_xO_y/Au)[2]. These devices show analog switching behavior, a high resistance and a strong I-V-nonlinearity, making them good candidates for the presented pattern recognition system. Aside from general pattern recognition performance, the impact of imperfect devices for the recognition rate will be shown. This includes the whole range of fabrication problems from shorted devices to devices with a high variability in switching, over to non-switching high resistance devices. Financial support by the German Research Foundation through FOR 2093 is gratefully acknowledged.

[1] F. Zahari et al., AIMS Materials Science 2: 203-216 (2015)
[2] M. Hansen et al., Scientific Reports, vol. 5, p. 13753 (2015)

DS 40.4 Thu 16:15 CHE 89

A Concentrated Model of the Double Barrier Memristive Device for LTSpice Simulations — •Enver Solan[1], Sven Dirkmann[2], Martin Ziegler[3], Mirko Hansen[3], Hermann Kohlstedt[3], Thomas Mussenbrock[4], and Karlheinz Ochs[1] — [1]Ruhr-Universität Bochum, Lehrstuhl für Digitale Kommunikationssysteme, 44780 Bochum — [2]Ruhr-Universität Bochum, Lehrstuhl für Theoretische Elektrotechnik, 44780 Bochum — [3]Nanoelektronik, Technische Fakultät, Christian-Albrechts-Universität zu Kiel, 24143 Kiel — [4]Brandenburgische Technische Universität Cottbus-Senftenberg, Fachgebiet Theoretische Elektrotechnik, 03046 Cottbus

The double barrier memristive device is a technical implementation of a memristive system. It consists of an ultra-thin memristive layer sandwiched between a tunnel barrier and a Schottky-like contact. In principle, it is a nonlinear resistor with memory, whereby the resistance depends on energetic states at the interfacial barriers. This leads to a continuous resistance range, which is desired for neuromorphic applications. To understand the underlying physical and chemical phenomena, a distributed model of the device, using a kinetic Monte-Carlo simulation, has been implemented. Such simulations are very time-consuming and therefore not suitable for real-time implementations, e.g. for emulation purposes. Starting from the distributed model a concentrated model of the device with physically meaningful parameters has been developed. It can be used for reproducible analyses and emulation purposes. The concentrated model was verified by comparisons with Monte-Carlo simulations as well as with measurements.

DS 40.5 Thu 16:30 CHE 89

An FPGA Implementation of a Memristive System Based on Wave Digital Principles — •Enver Solan[1], Benedikt Janssen[2], Karlheinz Ochs[1], and Michael Hübner[2] — [1]Ruhr-Universität Bochum, Lehrstuhl für Digitale Kommunikationssysteme, 44780 Bochum — [2]Ruhr-Universität Bochum, Lehrstuhl für Eingebettete Systeme der Informationstechnik, 44780 Bochum

The massively parallel structure of neuromorphic circuits leads to efficient computations of complex problems. Depending on the learning process, the interconnections between neurons are differently weighted. This functionality can be modeled by memristive devices * nonlinear resistors with memory.

These devices in nanotechnology contain always parameter spread, which makes reproducible analyses hard. Additionally, some neuro-

morphic applications may need a desired but not realizable memristive functionality. Simulation models can be used, but they are very time-consuming and even less suited for hardware emulation purposes. Due to these issues, hardware emulators of memristive systems are needed.

Our approach pursues an FPGA implementation of memristive systems based on wave digital principles. This leads to a generic memristive emulator by maintaining the passivity of the analog device.