DS 10 FV-internes Symposium Anorganische Dielektrika für die künftige Mikro- und Nanotechnologie

Zeit: Samstag 10:00–13:45 Raum: TU H110

Hauptvortrag DS 10.1 Sa 10:00 TU H110

Atomic-scale properties of high-k dielectrics for CMOS: ab initio study for Pr-based materials — •Jarek Dabrowski[1] and Andrzej Fleszar[2] — [1]IHP, Im Technologiepark 25, 15236 Frankfurt(Oder), Germany — [2]Universität Würzburg, Am Hubland, 97074 Würzburg, Germany

In the nearest future, a dielectric with a dielectric constant k several times higher than that of SiO_2 will be needed for the fabrication of CMOS devices. The search for an optimal dielectric is not complete. Numerous metal oxides and silicates are being investigated, various deposition and annealing techniques are being developed which try to utilize the effects attributed to alloying, incorporation of nitrogen, gettering of oxygen, etc. At the same time, the basic knowledge on the microscopic properties of these materials is poor. Ab initio calculations assist in the interpretation of the experimental results and in the choice of the direction of further work.

Using Pr-based dielectrics as a case study, we discuss the atomic and electronic structures of bulk oxides and silicates, of various defects and impurities, and of the interfaces to Si. We consider the native defects (vacancies and self-interstitials), the defects associated with such elements as Si, Ti, Sr, or B, the effect of moisture, and the diffusion of elements and moieties (e.g., of SiO_2 in Pr_2O_3). We describe the interaction between materials during fabrication of a dielectric film, e.g., the formation of electrically active defects in SiO_2 by a Pr layer deposited on top of a SiO_2 layer. Finally, we turn our attention to the formation of the interface between Si(001) and the Pr oxide and/or silicate.

Hauptvortrag DS 10.2 Sa 10:45 TU H110

Epitaxial growth of oxide layers on silicon surfaces — •Wolfgang Moritz[1], Nicole Jeutter[1], Laure Libralesso[2], and Jörg Zegenhagen[2] — [1]Dept. of Earth and Environmental Sciences, LMU München — [2]ESRF, Grenoble, France

In the search for high-k dielectrics to replace the SiO_2 layer in silicon based devices only few materials have been found so far. The oxides have to be thermodynamically stable in contact with Si at temperatures up to 1000° C and the formation of interfacial SiO_2 layers has to be avoided. Among the possible materials are oxides with the perowskite type structure, $Ba/SrTiO_3$ and rare earth oxides like Pr_2O_3, Y_2O_3 and CeO_2. The current status of the growth of epitaxial oxide layers is reviewed. Most promising is Pr_2O_3 which forms well ordered epitaxial layers on the Si(111) surface and which can be overgrown by Si. Results from X-ray diffraction and LEED show the initial stages of growth and an SiO_2 free interface structure. On the (100) surface the growth of oxide layers in general leads to layers with lower crystalline quality due to rotational domains. These are avoided on the Si(113) surface and first results for growth studies of Pr_2O_3 on this substrate orientation are presented. A further promising field seems to be the growth of layers of ternary oxides which have rarely been studied up to now, except for the perowskite type structures. First results for the growth of aluminosilicates are presented.

Hauptvortrag DS 10.3 Sa 11:30 TU H110

The role of interfaces in nanosize ferroelectrics oxides — •Marin Alexe, Lucian Pintilie, and Dietrich Hesse — Max-Planck-Institut für Mikrostrukturphysik, Weinberg 2, 06120 Halle

Multifunctional ferroelectric oxide materials offer a wide range of useful properties from switchable polarization that can be applied in memory devices to piezoelectric and pyroelectric properties used in actuators, transducers and thermal sensors. Generally speaking at the nanometer scale material properties are expected to be different. Fundamental problems such as the super-paraelectric limit, the influence of the free surface, and of the interface and bulk defects on ferroelectric switching, etc. arise when scaling down ferroelectrics. In order to study these size effects, fabrication methods of high quality nanoscale ferroelectric crystals have been developed. The present talk will briefly review self-patterning and self-assembly fabrication methods, including chemical routes, morphological instability of ultrathin films, microemulsion, and self-assembly lift-off, employed up to the date to fabricate ferroelectric nanoscale structures with lateral size in the range of few tens of nanometers. In depth structural and electrical investigations of interfaces performed to differentiate between intrinsic and extrinsic size effects will also be presented.

Hauptvortrag DS 10.4 Sa 12:15 TU H110

DRAM capacitor scaling — •M. Gutsche[1], T Hecht[1], S Jakschik[2], C Kapteyn[2], G Krautheim[2], S Kudelka[2], J Lützen[2], A Sänger[2], U Schröder[2], H Seidl[2], A Avellan[2], J Heitmann[2] und G Hirt[2] — [1]Infineon Technologies — [2]Ifx

Über viele Jahre hinweg hat die DRAM-Industrie wesentlich zum Fortschritt bei der Miniaturisierung mikroelektronischer Bausteine beigetragen. Um auch weiterhin bei kleiner werdenden lateralen Strukturgrößen und innovativen Zelldesigns eine genügend hohe Zellkapazität einer einzelnen Speicherzelle zur Verfügung stellen zu können, sind innovative Konzepte in den Bereichen Zellenlayout, Kondensatorgeometrie sowie Materialauswahl erforderlich. Stapel- und Grabenkondensatoren werden zunehmend höhere Aspektverhältnisse aufweisen, woraus sich zusätzliche Anforderungen an Ätz- und Abscheidungsverfahren ergeben. Die einzelnen Kondensatoren sind so anzuordnen, dass sie den Raum optimal ausfüllen und zugleich ihre mechanische Stabilität verbessert wird. Durch geeignete laterale Aufweitung von Strukturen sowie durch Oberflächenaufrauhung kann zusätzlich Kapazität bereitgestellt werden. Vor allem aber ist es notwendig, dielektrische Materialien mit größerer dielektrischer Konstante zum Einsatz zu bringen. In Verbindung mit metallischen Elektroden können MIS- und MIM-Strukturen hergestellt werden, mit deren Hilfe sich signifikant kleinere äquivalente Oxiddicken realisieren lassen.

Hauptvortrag DS 10.5 Sa 13:00 TU H110

Advance MOSFET gate dielectrics for high-performance microprocessors: Materials selection and analytical challenges — •E. Zschech[1], H.-J. Engelmann [1], K. K Dittmar [1], S. Ohsiek [1], B. Tracy[2], E. Adem [2], A. Myers[2], S. Robie [2], M. Sidorov [2], and J. Bernard [2] — [1]AMD Saxony LLC & Co. KG, Dresden, Germany — [2]Spansion Inc., Sunnyvale/CA, U. S.

According the 2003 ITRS roadmap [1], high-performance microprocessors (HP-MPUs) are driving the continuous shrinking of metal-oxide-semiconductor (MOS) feature sizes. The scal-ing down of the HP-MPU physical gate length follows a two-year cycle with a scaling factor of 0.7 until 2005 and switches to a three-year cycle thereafter, leading to 10 nm gates in 2015. The traditional down-scaling of MOS transistors leads to performance limitations that have to be overcome by the introduction of new materials in the gate stack, which result in new and exciting challenges to solid-state physicists and materials scientists. For leading edge logic products, the transistor performance can be further increased by metal oxide gate dielectrics with a high dielectric constant (high-k materials). The particular need for low-leakage devices is driving the implementation of high-k gate dielectric materials during the next couple of years - one of the key challenges for materials research and process inte-gration. However, until real high-k dielectrics will be introduced into the CMOS process, sili-con oxynitrides will being used as an interim solution. In this paper, material transitions that are necessary to improve the product performance and to maintain the product reliability of HP-MPUs are highlighted. Particularly, the reduction of gate leakage currents by the implementation of high-k materials (at first silicon oxynitrides, followed by metal oxides) for gate dielectrics in MOS transistors is discussed. The need of leading-edge analytics for the study of fundamental integration, performance and reliability issues of metal oxides and for the optimization silicon oxynitride thin films is demonstrated.

[1] International Technology Roadmap for Semiconductors (ITRS): Semiconductor Interna-tional Association (SIA), 2003 Edition, http://public.itrs.net