NICHTFLÜCHTIGE FESTKÖRPERSPEICHER (SYFS)

gemeinsam veranstaltet von den Fachverbänden
Dielektrische Festkörper (DF)
Dünne Schichten (DS)
Halbleiter (HL) und
Magnetismus (MA)

Organisation
D. Hesse (Halle) und G. Reiss (Bielefeld)

Kontakt
Dietrich Hesse
MPI für Mikrostrukturphysik
Weinberg 2
D-06120 Halle
E-Mail: hesse@mpi-halle.de

ÜBERSICHT DER HAUPTVORTRÄGE UND FACHSITZUNGEN

(Hörsaal TU HE101)

Hauptvorträge

SYFS 1.1	Sa	14:00	(TU HE101)	**Physical aspects and technical prospects of nonvolatile memories**, Heinrich Kurz
SYFS 2.1	Sa	14:45	(TU HE101)	**Nanoscopic control of the polarization in ferroelectric thin films**, J.-M. Triscone, P. Paruch, T. Tybell, N. Stucki, M. Dawber, T. Giamarchi
SYFS 3.1	Sa	15:45	(TU HE101)	**Status and outlook of MRAM technology**, Gill Yong Lee

Fachsitzungen

SYFS 1	**Overview, phase change and nanocrystal memories**	Sa 14:00–14:45	TU HE101	SYFS 1.1–1.2
SYFS 2	**Ferroelectric and dielectric memories**	Sa 14:45–15:45	TU HE101	SYFS 2.1–2.3
SYFS 3	**Magnetic memories**	Sa 15:45–16:30	TU HE101	SYFS 3.1–3.2
SYFS 4	**Poster**	Sa 08:30–16:30	Poster TU C	SYFS 4.1–4.9

Fachsitzungen

– Haupt-, Kurzvorträge und Posterbeiträge –

SYFS 1 Overview, phase change and nanocrystal memories

Zeit: Samstag 14:00–14:45 Raum: TU HE101

Hauptvortrag SYFS 1.1 Sa 14:00 TU HE101

Physical aspects and technical prospects of nonvolatile memories — •Heinrich Kurz — Institute of Semiconductor Electronics, RWTH Aachen University, Germany

Retaining data for years when unpowered is crucial for the most handheld electronic communication systems. Today non-volatile memories are dominated by flash concepts with various derivatives. Flash memories will face severe technological problems approaching the 65 nanometer technology node. Among the alternatives PC-RAM appears particularly attractive from physical point of view. Principally the performance of non-volatile memory should improve when the cell size is scaled down beyond the 65 nanometer node. In this talk the physical aspects and technical prospects of the PC-RAM technology will be discussed. In addition self-organization phenomena, recently explored for fabrication of highly dense nanostructures, are shown to open the way to extensions of current technologies towards extremely high storage densities. Examples in the field of quantum dot flash-memories and magnetic mass storage systems will be given.

SYFS 1.2 Sa 14:30 TU HE101

Fabrication of Si nanocrystals for memory application by ion irradiation through SiO_2/Si-interfaces — •B. Schmidt[1], K.-H. Heinig[1], L. Röntzsch[1], A. Mücklich[1], K.-H. Stegemann[2], E. Votintseva[2], and M. Klimenkov[3] — [1]Research Center Rossendorf, Dresden — [2]ZMD AG, Dresden — [3]Research Center Jülich, Jülich

This contribution addresses self-assembling of Si-nanocrystals (NCs) in gate oxides, with special emphasis on size and position tailoring and their application as discrete charge storage centers in nanocrystal memories. The Si NCs for these multi-dot floating-gate memories have been produced by ion irradiation through SiO_2/Si-interfaces. Si excess within SiO_2 is formed by ion beam mixing of Si from the Si substrate and from the poly-Si capping layer into the gate oxide. Ion irradiation with $3x10^{15} - 1x10^{16}$ Si^+ cm^{-2} at 50-100 keV through 50 nm poly-Si and 15 nm SiO_2 on (001)Si results in a considerable Si excess. At the upper and lower interfaces of the gate oxide, this ion irradiation forms a metastable SiO_x composition. Si NCs are formed by phase separation into Si and SiO_2 during post-irradiation thermal treatment. Adjacent to the recovering interfaces, narrow SiO_2 zones becomes denuded of excess Si. More distant excess Si precipitates as Si NCs in the gate oxide. This approach was applied to nMOSFET-NC-memory fabrication in the standard CMOS line at ZMD. MOSFET characteristics in terms of write/erase voltage, duration of the programming time, endurance and retention have been evaluated.

SYFS 2 Ferroelectric and dielectric memories

Zeit: Samstag 14:45–15:45 Raum: TU HE101

Hauptvortrag SYFS 2.1 Sa 14:45 TU HE101

Nanoscopic control of the polarization in ferroelectric thin films — •J.-M. Triscone[1], P. Paruch[1], T. Tybell[2], N. Stucki[1], M. Dawber[1], and T. Giamarchi[1] — [1]DPMC, University of Geneva, 24 Quai E.-Ansermet, 1211 Geneva 4, Switzerland — [2]NTNU, Trondheim, Norway

Ferroelectric memories take advantage of the non-volatile reversible nature of the ferroelectric polarization. In this work, we combine high quality materials, epitaxial atomically smooth ferroelectric perovskite films, and atomic force microscopy (AFM) to control and modify the ferroelectric domain structure at nanoscale. This approach allows new fundamental studies of ferroelectrics at nanoscale and might be a way to develop ultra-high density non-volatile memories. In ferroelectric $Pb(Zr_{0.2}Ti_{0.8})O_3$ thin films, a metallic AFM tip was used as a local electric field source to study individual nanoscale ferroelectric domains. Control of domain size was achieved by varying the strength and duration of the voltage pulses used to polarize the material, permitting the creation of sub-20nm wide lines and ultra-high density arrays reaching ∼30 Gbit/cm^2. The AFM approach developed also allowed us to investigate switching dynamics in ferroelectric thin films. Our data suggest a two step process of domain growth, in which initial nucleation under the AFM tip is followed by radial domain wall motion, perpendicular to the polarization direction. The electric field dependence of the domain wall velocity demonstrates that this motion is a creep process.

SYFS 2.2 Sa 15:15 TU HE101

First-principles theory of interfacial electronic structures and energy barriers in electroceramic thin-film devices — •Christian Elsässer[1], Matous Mrovec[1], Jan-Michael Albina[1], and Bernd Meyer[2] — [1]Fraunhofer-Institut für Werkstoffmechanik IWM, Wöhlerstr. 11, 79108 Freiburg — [2]Lehrstuhl für Theoretische Chemie, Ruhr-Universität, Universitätsstr. 150, 44780 Bochum

Nanostructured thin-film devices on the basis of electroceramic perovskite-type oxides have very promising structural, physical and chemical properties for highly integrated functional components, e.g., in computer technology, like high-density dynamic random access memory (RAM) made of $(Ba,Sr)TiO_3$, or novel non-volatile ferroelectric $Pb(Zr,Ti)O_3$ RAM devices. Critical issues in such systems are the interfacial structure, adhesion and electrical barriers at the contacts of the electroceramic thin films to conducting electrodes (e.g., Pt, $SrRuO_3$), and to insulating substrates (e.g., $SrTiO_3$, $LaAlO_3$).

First-principles electronic-structure calculations, by density functional theory and the mixed-basis pseudopotential method, were carried out to analyse interfacial Schottky barriers and band offsets at planar and coherent perovskite/metal and perovskite/perovskite contacts. Influences of different electrode materials, varying chemical film compositions and interface terminations on the interfacial energy barriers will be discussed.

This work is supported by the German Research Foundation (DFG) within the Priority Program "Integrated electroceramic functional structures".

SYFS 2.3 Sa 15:30 TU HE101

Resistive switching in $Ba_{0.7}Sr_{0.3}TiO_3$ thin films — •Rob Oligschlaeger[1], Silvia Karthäuser[2], Regina Dittmann[2], Kristof Szot[2], Rene Meyer[2], and Rainer Waser[1,2] — [1]Institut für Werkstoffe der Elektrotechnik 2, RWTH Aachen University, Germany — [2]CNI, Dept. IFF, Research Center Jülich, Germany

Recently, resistive switching of dielectric perovskite-type thin films has attracted a lot of attention in view of its potential for non-volatile information storage in future generation high speed random access memories [1]. We investigated resistive switching of capacitor-like thin film structures of $Ba_{0.7}Sr_{0.3}TiO_3$ (BST), prepared by pulsed laser deposition. $SrRuO_3$ (SRO) grown on (001) oriented $SrTiO_3$ substrates was used as bottom electrode. Pt top electrodes were deposited by sputtering. Electrical measurements show stable hysteretic behaviour in the current-voltage

curve. Positive or negative voltage pulses are employed to switch the resistance of the oxide films between a low- and a high-impedance state. The temperature dependence of the current in both states was determined. Read-write measurements over 10^4 cycles show some fatigue in the resistance states. Utilizing different write voltages for the pulses we achieved stable multilevel switching of the resistance. We will discuss the dopant dependence and the potential physical mechanism of the switching phenomena.

[1] A. Beck, J. G. Bednorz, Ch. Gerber, C. Rossel and D. Widmer, Appl. Phys. Lett. 77, 139 (2000)

SYFS 3 Magnetic memories

Zeit: Samstag 15:45–16:30 Raum: TU HE101

Hauptvortrag SYFS 3.1 Sa 15:45 TU HE101

Status and outlook of MRAM technology — •Gill Yong Lee — Infineon Technologies / Altis Semiconductor, 224 Bd John Kennedy, 91105 Corbeil Essonnes, France

This presentation reviews the current status of MRAM (Magnetoresistive Random Access Memory) technology and its outlook. In the MRAM devices, information is stored in terms of different magnetic orientation of a soft ferromagnetic layer with respect to a fixed reference layer. There are two different flavours of MRAM cells: The FET cell and the cross point cell. The FET cell uses an access transistor connected in series with the tunnel junction. Up until now, 16Mb MRAM is the highest density employing the FET cell with a 1.4 square micron cell size based on 0.18 micron Cu CMOS technology. On the other hand, with the cross point cell one can realize a very dense memory, since it does not require an access device. In addition, the cross point cell can be stacked on top of each other for even higher density. To control parasitic currents and the write operating margin, however, it requires a higher tunnel junction resistance than the FET cell, resulting in a slower random access time.
In general, the FET MRAM cell can be built with three additional masks relative to standard logic process: (i) the first mask layer for shallow via connection from the access transistor to the bottom of the magnetic tunnel junction (MTJ) stack; (ii) the second mask layer for the storage layer and the top electrode patterning; and (iii) the third mask layer for the patterning of the reference layer and the bottom electrode. Later, the top electrode can be connected to the upper Cu wiring level. The key process steps are the MTJ stack deposition on a very smooth surface after forming the shallow via, patterning of the MTJ stack, and its encapsulation after patterning. The manufacturing compatible MRAM integration scheme based on the processes that we developed provides sufficiently high write and read operation margins that are essential for the yielding memory chips.
In the cross point cell, the magnetic stack is first deposited directly on Cu wires, and then patterned by a single step reactive ion etching process that requires stopping on Cu and dielectrics without corrosion. The customized full stack etch process leads to MTJ patterning with a small local cell resistance spread.
The magnetoresistance (MR), the important figure of merit for the READ operation, was limited to 70 percent in the past. Recently, MTJ stack with a very high MR up to 220 percent has been reported by Infineon / IBM with 100 bcc textured MgO tunnel barriers. Higher MR will greatly increase the read operation margin and enable us to fabricate very small MTJs that are essential for scalability.

SYFS 3.2 Sa 16:15 TU HE101

From self-ordering towards imprint lithography: Large scale periodic nickel and permalloy nanowire arrays — •Kornelius Nielsch[1], Woo Lee[1], Ulrich Gösele[1], Ralf B. Wehrspohn[2], David Navas [3], and Manuel Vázquez[3] — [1]Max Planck Institute of Microstructure Physics, Halle — [2]Department of Physics, University of Paderborn — [3]Instituto de Ciencia de Materiales de Madrid, CSIC, Cantoblanco, Spain

In recent years magnetic arrays have attracted a lot of interest due to their potential application for perpendicular patterned magnetic media. Ni and Ni80Fe20 nanowires have been used due to the small magnetocrystalline anisotropy and a large anisotropy resulting from the wire shape. We will analyze the impact of the nanowire arrangement on the total anisotropy of the magnetic arrays and the deviation of the switching fields of individual nanowire with a disordered, polycrystalline and monocrystalline nanowire arrangement. Self-ordered alumina pore channel arrays are used partly as templates for the fabrication of magnetic nanowire arrays with a periodicity of 65, 100, and 500 nm. In analogy to polycrystallites, the nanowires are hexagonally arranged in domains, which are extended over more than ten lattice periods. We obtain a perfect hexagonal or monocrystalline arrangement on a cm2-scale, when we introduce imprint lithography in the fabrication process of our magnetic arrays. We observe that the total magnetic anisotropy increases by either reducing the deviation in nanowire diameter or by improving the ordering of the nanowire arrangement.

SYFS 4 Poster

Zeit: Samstag 08:30–16:30 Raum: Poster TU C

SYFS 4.1 Sa 08:30 Poster TU C

Reduction of azimuthal domains in (100)- and (118)-oriented ferroelectric $Bi_{3.25}La_{0.75}Ti_3O_{12}$ films making use of YSZ and Si substrates with definite off-cut — •Sung Kyun Lee[1], Ho Nyung Lee[2], and Dietrich Hesse[1] — [1]Max-Planck-Institut für Mikrostrukturphysik, D-06120 Halle (Saale), Germany — [2]Condensed Matter Science Division, Oak Ridge National Laboratory, TN 37831, USA

La-substituted bismuth titanate is a candidate for non-volatile ferroelectric RAMs, combining a high remanent polarization Pr with a very good fatigue resistance. Uniformly oriented $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) films have been grown by pulsed laser deposition. a-axis oriented BLT films on $SrRuO_3$(110)- electroded, YSZ(100)-buffered Si(100) wafers show a Pr of 32 microCoulomb/sqr-cm and a small fatigue of less than 10 percent after a billion cycles. Since (110)-oriented $SrRuO_3$ electrode layers grow on YSZ(100) buffer layers with four azimuthal domains, the BLT films consist of eight azimuthal domains involving 20°-, 70°- and 90°-domain boundaries. To reduce the number of azimuthal domains, $SrRuO_3$ layers and BLT films were grown by PLD onto YSZ(100) and YSZ(100)-buffered Si(100) single crystal substrates having a definite offcut. The offcut angle was varied from zero to 5° in steps of 1...2°; two azimuthal offcut directions were used, viz. [100] and [110]. The films were investigated by XRD pole figures and Phi scans, TEM, and ferro-electric measurements. A [110] offcut allowed to effectively reduce the number of domains and domain boundaries by 50 percent.

SYFS 4.2 Sa 08:30 Poster TU C

Asymmetric ferroelectric polarization loops and offset in Pt-ZnO-$BaTiO_3$-Pt thin film capacitor structures — •Nurdin Ashkenov, Mathias Schubert, Evgeni Twerdowski, Nirav Barapatre, Holger v. Wenckstern, Holger Hochmuth, Michael Lorenz, Wolfgang Grill, and Marius Grundmann — Fakultät für Physik und Geowissenschaften, Institut für Experimentelle Physik II, Universität Leipzig, Linnéstraße 5, 04103 Leipzig, Germany

Electric polarisation, current-voltage and capacitance-voltage studies on a wurtzite-perovskite-type metal/semiconductor/ferroelectric/metal heterostructure (Pt-ZnO-$BaTiO_3$-Pt), grown by pulsed laser deposition on (001)Si are reported. Strongly asymmteric polarization hysteresis loops with rectifying behavior are observed. The polarization value in the negative half of the hysteresis loop is larger than that in the positive half of the loop, and hysteresis loops shift along the polarization axis with increasing sweeping voltage. The origin of the hysteresis loop offsets and asymmetry is discussed and modeled in terms of space-charge region, leakage currents, and coupling between spontaneous wurtzite and switchable ferroelectric polarization.

SYFS 4.3 Sa 08:30 Poster TU C

Charakterisierung der elektrischen Eigenschaften von Chalkogeniden als Datenspeicher — •Hajo Noerenberg, Ralf Detemple und Matthias Wuttig — I. Physikalisches Institut IA, RWTH Aachen

Zur Zeit werden mehrere alternative Verfahren zur nicht-flüchtigen und schnellen elektronischen Speicherung diskutiert. Eine der erfolgversprechendsten Methoden basiert auf der Technologie der Phase-Change-Materialien (PCRAM). Hierbei wird ausgenutzt, dass diese Materialien je nach Phasenzustand einen deutlichen Unterschied der Leitfähigkeit vorweisen. Das Umschalten der Phasen wird durch Strompulse geeigneter Stärke und Dauer angeregt, welche die Probe lokal aufheizen. In Abhängigkeit von der erreichten Temperatur und der Abkühlrate wechselt das Material in den kristallinen oder amorphen Zustand, in welchem es nach Ende des Pulses verbleibt (non-volatile memory).

Es wird die Strukturierung und Kontaktierung einer Speichereinheit (Bit) auf einer durch Magnetronsputtern hergestellen Probe vorgestellt. Für verschiedene ternäre und quaternäre Tellurverbindungen wurde die Kinetik der Phasenumschaltung untersucht.

SYFS 4.4 Sa 08:30 Poster TU C

CMOS-compatible multi-dot floating-gate non-volatile memory fabrication by ion beam processing — •K.-H. Heinig[1], B. Schmidt[1], T. Müller[1], C. Bonafos[2], A. Claverie[2], K.-H. Stegemann[3], E. Votintseva[3], P. Normand[4], P. Dimitrakis[4], E. Kapetanakis[4], M. Perego[5], M. Fanciulli[5], and V. V.Soncini[6] — [1]Forschungszentrum Rossendorf, Dresden, Germany — [2]CEMES/CNRS, Toulouse, France — [3]ZMD, Dresden, Germany — [4]IMEL, NCSR Demokritos, Athens, Greece — [5]MDM-INFM, Agrate, Italy — [6]Central R&D STMicroelectronics, Agrate, Italy

Conceptual, the replacement of floating poly-Si gates in current flash RAMs by Si nanocrystal (NC) layers leads to considerable improvements: Single tunnel oxide defects lead not to complete de-charging of floating gates, i.e. thinner tunnel oxides are possible which allows charging by direct tunnelling, resulting in better endurence, faster operation and lower write voltage of memories. Thus, due to this small modification of current non-volatile memories the performance might be improved substantially. The fabrication of such narrow Si NC layers is a challenge to materials research. Within an EU project with leading industry involved, we showed that this structure can be achieved by ion beam processing. Two approaches were studied, (i) low-energy ($\approx 1keV$) Si^+ ion implantation in gate oxides and (ii) ion beam mixing of (001)Si/oxide/poly-Si stacks by high-energy ($\approx 100keV$) Si^+ ion irradiation. Both processes are CMOS-compatible, and with each process non-volatile memories have been fabricated. The memory characteristics are very promising. Here we will focus on NC layer fabrication.

SYFS 4.5 Sa 08:30 Poster TU C

Ion irradiation through SiO_2-Si interfaces: TEM study of self-organized Si nanocrystals applicable in nonvolatile memories — •Lars Röntzsch, Karl-Heinz Heinig, and Bernd Schmidt — Research Center Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden

In recent years, immense effort has been devoted to the synthesis of Si nanocrystals (NCs) for multi-dot floating-gate MOSFETs. To assure optimum memory device characteristics, the Si NCs should be equal in size and equally distant from the transistor channel. This desired Si NCs structure can be fabricated in a two-step process of ion irradiation through a SiO_2-Si interface and subsequent annealing [1,2]. Previously, the Si NCs could not directly been studied with XTEM because of the low mass contrast of Si NCs to SiO_2 and their very small size of less than 3nm.

In this XTEM study we prove the validity of the Si NC formation process. For a mass contrast enhancement of the Si NCs we used Ge to decorate them: A thin Ge layer was embedded into the oxide. During annealing, diffusing Ge is captured by the Si NCs due to the favourable Si-Ge bond. Thereby, the Si NCs are alloyed resulting in $Si_{1-x}Ge_x$ NCs which are equally aligned with the SiO_2-Si interface in a tunnel distance of about 3nm. These structural results are in line with the eletronic device characteristics which are dicussed in the contributions of Heinig and Schmidt in this symposium.

[1] Heinig et al., Appl. Phys. A77, 17 (2003)

[2] Röntzsch et al., submitted to Appl. Phys. Lett.

SYFS 4.6 Sa 08:30 Poster TU C

Resistive switching in ferroelectric materials — •Hermann Kohlstedt[1], Adrian Petraru[1], René Meyer[1], Nicholas Pertsev[2], Ulrich Poppe[1], and Rainer Waser[1] — [1]Forschungszentrum Jülich GmbH, Institut für Festkörperforschung and CNI, Germany — [2]A. F. Ioffe Physico-Technical Institute, 194021 St. Petersburg, Russia

We present a model and experimental results for a novel ferroresistive switching device for non-volatile memory applications with a non-destructive read-out scheme. The device compromises a metal-dielectric-ferroelectric-metal layer sequence in which the dielectric and ferroelectric films are considered to be slightly conductive. We show that the resistance of this devices depends on the polarization state of the ferroelectric material. Experimental results on SRO/PZT(50/50)/Pt and SRO/PZT(20/80)/Pt mesa structures show indeed two resistive branches which can be reached by applying sufficiently large voltage pulses. The result will be compared to recently published resistive switching effects observed in non-ferroelectric complex oxides layer structures. Moreover in a short overview on resistive switching in insulators we show how complex this phenomenon is and that resistive switching is far from being understood. Finally we present a method based on a conductive AFM in the contact mode, to distinguish ferroelectric switching from non-ferroelectric resistive switching events by a simultaneous acquisition of d33 (V), C(V) and I (V).

SYFS 4.7 Sa 08:30 Poster TU C

Ferroelectric nanostructure arrays grown by PLD using metal nanotube membranes as deposition masks — •Sung Kyun Lee, Woo Lee, Marin Alexe, Kornelius Nielsch, and Dietrich Hesse — Max-Planck-Institut of Microstructure Physics Halle, Germany

Non-volatile ferroelectric random access memories (NV-FRAMs) with high memory density require the preparation of ferroelectric nanostructure arrays with a lateral size of the individual nanostructure in the range of 100 nm. Lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT) and lanthanum-substituted bismuth titanate $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) are the most favourable materials for this purpose. Well-oriented epitaxial nanostructures have the advantage of uniform ferroelectric cell-to-cell properties. Pulsed laser deposition (PLD) is a suitable method to grow well-oriented PZT and BLT films. Using deposition masks made from metal nanotube membranes, partially or fully well-oriented BLT and PZT nanostructure arrays have been prepared by PLD. Their structure and morphology are investigated by AFM, XRD pole figures, and (HR)TEM. The ferroelectric properties are determined by piezoresponse-scanning force microscopy (PFM). Well-developed ferroelectric hysteresis curves have been obtained from switchable nanostructures of about 100 nm lateral size.

SYFS 4.8 Sa 08:30 Poster TU C

Electrical behavior of size-controlled Si nanocrystals arranged as single layer — •Tiezheng Lu, Jun Shen, Marin Alexe, Roland Scholz, and Margit Zacharias — Max Planck Institute of Microstructure Physics, Weinberg.2 06120,Halle

A MOS structure was fabricated containing a single layer of size controlled Si nanocrystal. Size control was realized by using a SiO2/SiO/SiO2 superlattice with the embedded SiO layer having the thickness of the desired Si nanocrystals and using a 1100°C annealing to form the around 4 nm size Si nanocrystals. Current-voltage (I-V), capacitance-voltage (C-V) and conductance-voltage (G-V) were realized. From the Fowler-Nordheim plot an effective barrier height of 1.6 eV was estimated for our Si nanocrystals. A charge density of 3x1012/cm2 was measured which is in the range of the approximated Si nanocrystal density. The conductance method reveals a very low interface charge of our MOS structure. Electron trapping, storing, and de-trapping within the Si nanocrystals will be discussed based on the measurements.

SYFS 4.9 Sa 08:30 Poster TU C

Non-linear imprint behavior of ferroelectric PZT thin films — •P.J. Schorn, U. Böttger, and R. Waser — Institut für Werkstoffe der Elektrotechnik 2, RWTH Aachen University, Germany

Ferroelectric oxide thin film capacitors are promising candidates for non-volatile Ferroelectric Random Access Memories (FeRAMs) as they exhibit a switchable polarization. One of the most important failure-mechanisms of these capacitors is the imprint effect. In this contribution the imprint effect of $Pb(Zr_{0.3}Ti_{0.7})O_3$ (PZT) thin films is investigated. The most crucial failure due to imprint is the voltage shift expected during the runtime of the device. Taking a closer look at the static and

dynamic imprint reveals that the mean coercive voltage shift over the logarithmic value of elapsed time is non-linear. This is in contrast to the current imprint model in the literature that only explains a linear increase of the voltage shift over log(time). Hence, a simple linear fit will lead to a crucial error in the lifetime-estimations. Investigating the temperature dependence of the shift behavior within the single linear branches one can clearly calculate two different activation energies for the different regimes. The activation energies can be calculated to amount $W_A = 98$ meV for region I and $W_A = 44$ meV for region III. The possible physical nature of this imprint behaviour will be discussed.