SYFS 3 Magnetic memories

Zeit: Samstag 15:45–16:30 Raum: TU HE101

Hauptvortrag

SYFS 3.1 Sa 15:45 TU HE101

Status and outlook of MRAM technology — •Gill Yong Lee — Infineon Technologies / Altis Semiconductor, 224 Bd John Kennedy, 91105 Corbeil Essonnes, France

This presentation reviews the current status of MRAM (Magnetoresistive Random Access Memory) technology and its outlook. In the MRAM devices, information is stored in terms of different magnetic orientation of a soft ferromagnetic layer with respect to a fixed reference layer. There are two different flavours of MRAM cells: The FET cell and the cross point cell. The FET cell uses an access transistor connected in series with the tunnel junction. Up until now, 16Mb MRAM is the highest density employing the FET cell with a 1.4 square micron cell size based on 0.18 micron Cu CMOS technology. On the other hand, with the cross point cell one can realize a very dense memory, since it does not require an access device. In addition, the cross point cell can be stacked on top of each other for even higher density. To control parasitic currents and the write operating margin, however, it requires a higher tunnel junction resistance than the FET cell, resulting in a slower random access time.
In general, the FET MRAM cell can be built with three additional masks relative to standard logic process: (i) the first mask layer for shallow via connection from the access transistor to the bottom of the magnetic tunnel junction (MTJ) stack; (ii) the second mask layer for the storage layer and the top electrode patterning; and (iii) the third mask layer for the patterning of the reference layer and the bottom electrode. Later, the top electrode can be connected to the upper Cu wiring level. The key process steps are the MTJ stack deposition on a very smooth surface after forming the shallow via, patterning of the MTJ stack, and its encapsulation after patterning. The manufacturing compatible MRAM integration scheme based on the processes that we developed provides sufficiently high write and read operation margins that are essential for the yielding memory chips.
In the cross point cell, the magnetic stack is first deposited directly on Cu wires, and then patterned by a single step reactive ion etching process that requires stopping on Cu and dielectrics without corrosion. The customized full stack etch process leads to MTJ patterning with a small local cell resistance spread.
The magnetoresistance (MR), the important figure of merit for the READ operation, was limited to 70 percent in the past. Recently, MTJ stack with a very high MR up to 220 percent has been reported by Infineon / IBM with 100 bcc textured MgO tunnel barriers. Higher MR will greatly increase the read operation margin and enable us to fabricate very small MTJs that are essential for scalability.

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From self-ordering towards imprint lithography: Large scale periodic nickel and permalloy nanowire arrays — •Kornelius Nielsch[1], Woo Lee[1], Ulrich Gösele[1], Ralf B. Wehrspohn[2], David Navas [3], and Manuel Vázquez[3] — [1]Max Planck Institute of Microstructure Physics, Halle — [2]Department of Physics, University of Paderborn — [3]Instituto de Ciencia de Materiales de Madrid, CSIC, Cantoblanco, Spain

In recent years magnetic arrays have attracted a lot of interest due to their potential application for perpendicular patterned magnetic media. Ni and Ni80Fe20 nanowires have been used due to the small magnetocrystalline anisotropy and a large anisotropy resulting from the wire shape. We will analyze the impact of the nanowire arrangement on the total anisotropy of the magnetic arrays and the deviation of the switching fields of individual nanowire with a disordered, polycrystalline and monocrystalline nanowire arrangement. Self-ordered alumina pore channel arrays are used partly as templates for the fabrication of magnetic nanowire arrays with a periodicity of 65, 100, and 500 nm. In analogy to polycrystallites, the nanowires are hexagonally arranged in domains, which are extended over more than ten lattice periods. We obtain a perfect hexagonal or monocrystalline arrangement on a cm2-scale, when we introduce imprint lithography in the fabrication process of our magnetic arrays. We observe that the total magnetic anisotropy increases by either reducing the deviation in nanowire diameter or by improving the ordering of the nanowire arrangement.