SYFS 4 Poster

Zeit: Samstag 08:30–16:30 Raum: Poster TU C

SYFS 4.1 Sa 08:30 Poster TU C

Reduction of azimuthal domains in (100)- and (118)-oriented ferroelectric $Bi_{3.25}La_{0.75}Ti_3O_{12}$ films making use of YSZ and Si substrates with definite off-cut — •Sung Kyun Lee[1], Ho Nyung Lee[2], and Dietrich Hesse[1] — [1]Max-Planck-Institut für Mikrostrukturphysik, D-06120 Halle (Saale), Germany — [2]Condensed Matter Science Division, Oak Ridge National Laboratory, TN 37831, USA

La-substituted bismuth titanate is a candidate for non-volatile ferroelectric RAMs, combining a high remanent polarization Pr with a very good fatigue resistance. Uniformly oriented $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) films have been grown by pulsed laser deposition. a-axis oriented BLT films on $SrRuO_3$(110)- electroded, YSZ(100)-buffered Si(100) wafers show a Pr of 32 microCoulomb/sqr-cm and a small fatigue of less than 10 percent after a billion cycles. Since (110)-oriented $SrRuO_3$ electrode layers grow on YSZ(100) buffer layers with four azimuthal domains, the BLT films consist of eight azimuthal domains involving 20°-, 70°- and 90°-domain boundaries. To reduce the number of azimuthal domains, $SrRuO_3$ layers and BLT films were grown by PLD onto YSZ(100) and YSZ(100)-buffered Si(100) single crystal substrates having a definite offcut. The offcut angle was varied from zero to 5° in steps of 1...2°; two azimuthal offcut directions were used, viz. [100] and [110]. The films were investigated by XRD pole figures and Phi scans, TEM, and ferro-electric measurements. A [110] offcut allowed to effectively reduce the number of domains and domain boundaries by 50 percent.

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Asymmetric ferroelectric polarization loops and offset in Pt-ZnO-$BaTiO_3$-Pt thin film capacitor structures — •Nurdin Ashkenov, Mathias Schubert, Evgeni Twerdowski, Nirav Barapatre, Holger v. Wenckstern, Holger Hochmuth, Michael Lorenz, Wolfgang Grill, and Marius Grundmann — Fakultät für Physik und Geowissenschaften, Institut für Experimentelle Physik II, Universität Leipzig, Linnéstraße 5, 04103 Leipzig, Germany

Electric polarisation, current-voltage and capacitance-voltage studies on a wurtzite-perovskite-type metal/semiconductor/ferroelectric/metal heterostructure (Pt-ZnO-$BaTiO_3$-Pt), grown by pulsed laser deposition on (001)Si are reported. Strongly asymmteric polarization hysteresis loops with rectifying behavior are observed. The polarization value in the negative half of the hysteresis loop is larger than that in the positive half of the loop, and hysteresis loops shift along the polarization axis with increasing sweeping voltage. The origin of the hysteresis loop offsets and asymmetry is discussed and modeled in terms of space-charge region, leakage currents, and coupling between spontaneous wurtzite and switchable ferroelectric polarization.

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Charakterisierung der elektrischen Eigenschaften von Chalkogeniden als Datenspeicher — •Hajo Noerenberg, Ralf Detemple und Matthias Wuttig — I. Physikalisches Institut IA, RWTH Aachen

Zur Zeit werden mehrere alternative Verfahren zur nicht-flüchtigen und schnellen elektronischen Speicherung diskutiert. Eine der erfolgversprechendsten Methoden basiert auf der Technologie der Phase-Change-Materialien (PCRAM). Hierbei wird ausgenutzt, dass diese Materialien je nach Phasenzustand einen deutlichen Unterschied der Leitfähigkeit vorweisen. Das Umschalten der Phasen wird durch Strompulse geeigneter Stärke und Dauer angeregt, welche die Probe lokal aufheizen. In Abhängigkeit von der erreichten Temperatur und der Abkühlrate wechselt das Material in den kristallinen oder amorphen Zustand, in welchem es nach Ende des Pulses verbleibt (non-volatile memory).

Es wird die Strukturierung und Kontaktierung einer Speichereinheit (Bit) auf einer durch Magnetronsputtern hergestellen Probe vorgestellt. Für verschiedene ternäre und quaternäre Tellurverbindungen wurde die Kinetik der Phasenumschaltung untersucht.

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CMOS-compatible multi-dot floating-gate non-volatile memory fabrication by ion beam processing — •K.-H. Heinig[1], B. Schmidt[1], T. Müller[1], C. Bonafos[2], A. Claverie[2], K.-H. Stegemann[3], E. Votintseva[3], P. Normand[4], P. Dimitrakis[4], E. Kapetanakis[4], M. Perego[5], M. Fanciulli[5], and V. V.Soncini[6] — [1]Forschungszentrum Rossendorf, Dresden, Germany — [2]CEMES/CNRS, Toulouse, France — [3]ZMD, Dresden, Germany — [4]IMEL, NCSR Demokritos, Athens, Greece — [5]MDM-INFM, Agrate, Italy — [6]Central R&D STMicroelectronics, Agrate, Italy

Conceptual, the replacement of floating poly-Si gates in current flash RAMs by Si nanocrystal (NC) layers leads to considerable improvements: Single tunnel oxide defects lead not to complete de-charging of floating gates, i.e. thinner tunnel oxides are possible which allows charging by direct tunnelling, resulting in better endurence, faster operation and lower write voltage of memories. Thus, due to this small modification of current non-volatile memories the performance might be improved substantially. The fabrication of such narrow Si NC layers is a challenge to materials research. Within an EU project with leading industry involved, we showed that this structure can be achieved by ion beam processing. Two approaches were studied, (i) low-energy ($\approx 1keV$) Si^+ ion implantation in gate oxides and (ii) ion beam mixing of (001)Si/oxide/poly-Si stacks by high-energy ($\approx 100keV$) Si^+ ion irradiation. Both processes are CMOS-compatible, and with each process non-volatile memories have been fabricated. The memory characteristics are very promising. Here we will focus on NC layer fabrication.

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Ion irradiation through SiO_2-Si interfaces: TEM study of self-organized Si nanocrystals applicable in nonvolatile memories — •Lars Röntzsch, Karl-Heinz Heinig, and Bernd Schmidt — Research Center Rossendorf, Institute of Ion Beam Physics and Materials Research, Dresden

In recent years, immense effort has been devoted to the synthesis of Si nanocrystals (NCs) for multi-dot floating-gate MOSFETs. To assure optimum memory device characteristics, the Si NCs should be equal in size and equally distant from the transistor channel. This desired Si NCs structure can be fabricated in a two-step process of ion irradiation through a SiO_2-Si interface and subsequent annealing [1,2]. Previously, the Si NCs could not directly been studied with XTEM because of the low mass contrast of Si NCs to SiO_2 and their very small size of less than 3nm.

In this XTEM study we prove the validity of the Si NC formation process. For a mass contrast enhancement of the Si NCs we used Ge to decorate them: A thin Ge layer was embedded into the oxide. During annealing, diffusing Ge is captured by the Si NCs due to the favourable Si-Ge bond. Thereby, the Si NCs are alloyed resulting in $Si_{1-x}Ge_x$ NCs which are equally aligned with the SiO_2-Si interface in a tunnel distance of about 3nm. These structural results are in line with the eletronic device characteristics which are dicussed in the contributions of Heinig and Schmidt in this symposium.

[1] Heinig et al., Appl. Phys. A77, 17 (2003)
[2] Röntzsch et al., submitted to Appl. Phys. Lett.

SYFS 4.6 Sa 08:30 Poster TU C

Resistive switching in ferroelectric materials — •Hermann Kohlstedt[1], Adrian Petraru[1], René Meyer[1], Nicholas Pertsev[2], Ulrich Poppe[1], and Rainer Waser[1] — [1]Forschungszentrum Jülich GmbH, Institut für Festkörperforschung and CNI, Germany — [2]A. F. Ioffe Physico-Technical Institute, 194021 St. Petersburg, Russia

We present a model and experimental results for a novel ferroresistive switching device for non-volatile memory applications with a non-destructive read-out scheme. The device compromises a metal-dielectric-ferroelectric-metal layer sequence in which the dielectric and ferroelectric films are considered to be slightly conductive. We show that the resistance of this devices depends on the polarization state of the ferroelectric material. Experimental results on SRO/PZT(50/50)/Pt and SRO/PZT(20/80)/Pt mesa structures show indeed two resistive branches which can be reached by applying sufficiently large voltage pulses. The result will be compared to recently published resistive switching effects observed in non-ferroelectric complex oxides layer structures. Moreover in a short overview on resistive switching in insulators we show how complex this phenomenon is and that resistive switching is far from being understood. Finally we present a method based on a conductive AFM in the contact mode, to distinguish ferroelectric switching from non-ferroelectric resistive switching events by a simultaneous acquisition of d33 (V), C(V) and I (V).

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Ferroelectric nanostructure arrays grown by PLD using metal nanotube membranes as deposition masks — •Sung Kyun Lee, Woo Lee, Marin Alexe, Kornelius Nielsch, and Dietrich Hesse — Max-Planck-Institut of Microstructure Physics Halle, Germany

Non-volatile ferroelectric random access memories (NV-FRAMs) with high memory density require the preparation of ferroelectric nanostructure arrays with a lateral size of the individual nanostructure in the range of 100 nm. Lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT) and lanthanum-substituted bismuth titanate $Bi_{3.25}La_{0.75}Ti_3O_{12}$ (BLT) are the most favourable materials for this purpose. Well-oriented epitaxial nanostructures have the advantage of uniform ferroelectric cell-to-cell properties. Pulsed laser deposition (PLD) is a suitable method to grow well-oriented PZT and BLT films. Using deposition masks made from metal nanotube membranes, partially or fully well-oriented BLT and PZT nanostructure arrays have been prepared by PLD. Their structure and morphology are investigated by AFM, XRD pole figures, and (HR)TEM. The ferroelectric properties are determined by piezoresponse-scanning force microscopy (PFM). Well-developed ferroelectric hysteresis curves have been obtained from switchable nanostructures of about 100 nm lateral size.

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Electrical behavior of size-controlled Si nanocrystals arranged as single layer — •Tiezheng Lu, Jun Shen, Marin Alexe, Roland Scholz, and Margit Zacharias — Max Planck Institute of Microstructure Physics, Weinberg.2 06120,Halle

A MOS structure was fabricated containing a single layer of size controlled Si nanocrystal. Size control was realized by using a SiO2/SiO/SiO2 superlattice with the embedded SiO layer having the thickness of the desired Si nanocrystals and using a 1100°C annealing to form the around 4 nm size Si nanocrystals. Current-voltage (I-V), capacitance-voltage (C-V) and conductance-voltage (G-V) were realized. From the Fowler-Nordheim plot an effective barrier height of 1.6 eV was estimated for our Si nanocrystals. A charge density of 3x1012/cm2 was measured which is in the range of the approximated Si nanocrystal density. The conductance method reveals a very low interface charge of our MOS structure. Electron trapping, storing, and de-trapping within the Si nanocrystals will be discussed based on the measurements.

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Non-linear imprint behavior of ferroelectric PZT thin films — •P.J. Schorn, U. Böttger, and R. Waser — Institut für Werkstoffe der Elektrotechnik 2, RWTH Aachen University, Germany

Ferroelectric oxide thin film capacitors are promising candidates for non-volatile Ferroelectric Random Access Memories (FeRAMs) as they exhibit a switchable polarization. One of the most important failure-mechanisms of these capacitors is the imprint effect. In this contribution the imprint effect of $Pb(Zr_{0.3}Ti_{0.7})O_3$ (PZT) thin films is investigated. The most crucial failure due to imprint is the voltage shift expected during the runtime of the device. Taking a closer look at the static and dynamic imprint reveals that the mean coercive voltage shift over the logarithmic value of elapsed time is non-linear. This is in contrast to the current imprint model in the literature that only explains a linear increase of the voltage shift over log(time). Hence, a simple linear fit will lead to a crucial error in the lifetime-estimations. Investigating the temperature dependence of the shift behavior within the single linear branches one can clearly calculate two different activation energies for the different regimes. The activation energies can be calculated to amount W_A = 98 meV for region I and W_A = 44 meV for region III. The possible physical nature of this imprint behaviour will be discussed.