HL 35: Devices

Time: Thursday 10:00–12:45 Location: H13

HL 35.1 Thu 10:00 H13

Recent Advances in Complementary Tunneling FETs — •Martin Sterkel, Bernhard Fabel, Thomas Maul, Linda Nowack, and Walter Hansch — Institute for Technical Electronics, Technical University Munich, Arcisstr. 21, D-80333 München

Scaling MOSFETs becomes more and more difficult. The Tunneling Field Effect Transistor (TFET) is a possible successor of today's MOSFETs with high scaling capabilities.

The basic structure of the TFET is a reverse biased *pin*-diode with a MOS-gate on top of the intrinsic region. Depending on the applied gate-source voltage the electrical behaviour between the drain and the source contacts can be switched from the characteristics of a *pin*-diode to that of an Esaki diode. Hence, the working principle of a TFET is gate controlled interband tunneling. Both a positive and a negative gate-source voltage results in the formation of a tunnel junction, either on the *pi*- or the *ni*- interface. Therefore, complementary devices can be fabricated. Since the active region of the device has a lateral extension of approximately 10 nm, the TFET can be scaled down to less than 20 nm without severe short channel effects (SCE).

Planar TFETs were fabricated on silicon substrates by using standard CMOS technology. The p^+ source and n^+ drain regions were formed by Rapid Thermal Diffusion from Spin-On-Dopands. The fabrication process and the final devices are completely analyzed by using spectral ellipsometry, SIMS and various electrical measurement techniques. Selected results of these measurements are presented, discussed and compared with simulations.

HL 35.2 Thu 10:15 H13

MOSFET controlled Emission from Micro Field Emitter Tips — •Thomas Maul, Bernhard Fabel, Linda Nowack, Martin Sterkel, and Walter Hansch — Institute for Technical Electronics, Technical University Munich, Arcisstr. 21, 80333 Munich, Germany

Current stabilized field emitters are an ongoing subject to research and development for a couple of years, especially for flat panel displays. Alongside to this development field emitters are a promising candidate for economic multiplicative exposure of photo resists for nanostructures in future semiconductor manufacturing. As yet unrecoverable irregularities in manufacturing and resulting ageing of emitter tips during operation (e.g. combustion and adsorption of contaminations) lead to a drastic variance of emission between different tips and over time. So it is necessary to adjust the emission current in a different way. This submission shows ways to stabilize the current of field emitters by integrating emitter tips in drain contacts of MOSFETs and control the emission herewith. Experimental results are shown as well as simulations.

HL 35.3 Thu 10:30 H13

A non-volatile memory device based on self-organized quantum dots — •Andreas Marent, Martin Geller, David Feise, Konstantin Pötschke, and Dieter Bimberg — Institut für Festkörperphysik, TU Berlin, Hardenbergstr. 36, 10623 Berlin

DRAM and Flash are the most important semiconductor memories, both having their advantages and disadvantages in storage/access time and endurance. A future memory cell should combine the advantages of DRAM and Flash to an ultimate memory with long endurance (>10^{15} write/erase cycles), long storage time (>10 years), fast write/read access time (<1 ns) and scalability towards single electron functionality yielding ultimately small power consumption.

We present a memory concept based on self-organized quantum dots (QDs) with the potential to fulfill all requirements concerning storage/access time, endurance and scalability [1]. In InAs QDs with $Al_{0.9}Ga_{0.1}As$ we demonstrate a hole storage time of seconds at room temperature. Futher enhanced storage time up to 10 years is expected for different material combinations such as In(Ga)Sb in AlAs. Futhermore, an average time for hole capture and relaxation at room temperature of 0.3 ps is observed for InAs/GaAs QDs . Thus, in comparison to a DRAM cell, a four order of magnitude faster write time is possible in such a QD-based memory.

[1] M. Geller, A. Marent, and D. Bimberg, Auf Halbleiter-Nanostrukturen basierender nicht-flüchtiger Speicher "A non-volatile memory based on semiconductor nanostructure", CPT patent application, submitted (2006).

HL 35.4 Thu 10:45 H13

Geometrical spin dephasing in quantum dots — •Pablo San-Jose[1], Gergely Zarand[2], Alexander Shnirman[1], and Gerd Schön[1] — [1]Institut für Theoretische Festkörperphysik and DFG-Center for Functional Nanostructures (CFN), Universität Karlsruhe,D-76128 Karlsruhe, Germany. — [2]Institute of Physics, Technical University Budapest, Budapest, H-1521, Hungary.

We study the relaxation and dephasing of electron spins in quantum dots that is mediated by spin-orbit coupling, and show that higher order contributions provide a relaxation mechanism that dominates in the limit of low magnetic fields. This relaxation is of geometrical origin. We further observe that in the low-field limit the relaxation processes are dominated by coupling to electron-hole excitations rather than by phonons. We also consider the possibility of spin manipulation by spin-orbit induced geometric phases.

HL 35.5 Thu 11:00 H13

Silicon Epitaxy for vertical Tunnel Field-Effect-Transistors — •Markus Schindler, Oliver Senftleben, Mathias Born, Krishna Kumar Bhuwalka, Matthias Schmidt, and Ignaz Eisele — Institute of Physics, Department of Electrical Engineering, University of the German Federal Armed Forces Munich, Werner-Heisenberg-Weg 39, 85577 Neubiberg,Germany

The vertical tunnel field-effect-transistor (TFET) has been proposed as a candidate for future CMOS structures. The main features are exponentially increasing drain current-gate voltage characteristics and symmetric performance in n- and p-channel operation. Since the tunneling junction is less than 5 nm deposition processes with atomically sharp doping transitions are needed. Dopant diffusion and hence process temperature must be limited. Vertical TFET-structures were already grown by MBE, but a low-temperature CVD-based process suitable for an industrial production enviroment is still lacking. We investigated p- and n-type doped Si-layers grown in a commercial low pressure-CVD-system. The deposition temperature was under 650°C and the samples were characterized by secondary-ion-mass-spectroscopy (SIMS) and scanning electron microscopy (SEM). Deposition rates and doping incorporation show very high efficiency compared to conventional silane/dichlorosilane based epitaxy. As demonstrators we present experimental verification of p-channel tunnel FETs down to i-zones of 70 nm and 25 nm. I-V-characteristics are weakly dependent on temperature and nearly independent on channel length.

15 min. break

HL 35.6 Thu 11:30 H13

Characterisation of ultrathin ALD-Al_2O_3 films in MOS devices — •Bernhard Fabel[1], Martin Sterkel[1], Thomas Maul[1], Linda Nowack[1], Walter Hansch[1], Florian Speck[2], Kunyuan Gao[2], Thomas Seyller[2], and Lothar Ley[2] — [1]Institute for Technical Electronics, Technical University Munich, Arcisstr. 21, D-80333 München — [2]Institute for Technical Physics, University Erlangen-Nürnberg, Erwin-Rommel-Str. 1, D91058 Erlangen

We present to you a comprehensive study of the electrical impact of different precursors and post deposition treatments to the ALD system of aluminium oxide. These ultrathin (EOT < 2 nm) aluminium oxide Al_2O_3 films were fabricated with different secondary precursors in an standard ALD furnace. The focus was on ozon and water synthesised films as well as mixed processes using both precursors. The electrical parameters were obtained from MOS capacitances and MOSFET devices, leading to a complete evaluation of the film properties for future CMOS applications. Additional physical characterisations (TEM, XPS, etc.) allow to match the electrical behaviour with the microscopic structure of the films in dependence of depostion conditions.

HL 35.7 Thu 11:45 H13

Butted Source Contact Field Effect Transistor — •Marcus Weis, Michael Fulde, and Doris Schmitt-Landsiedel — Lehrstuhl für Technische Elektronik, TU München

With scaling technology and smaller feature sizes alternative transistor structures gain momentum as replacement or in addition to traditional CMOS technology. In this work we investigate a novel device, the But-

ted Source Contact Field Effect Transistor (BSC-FET).

An experimental BSC device was investigated with a structure similar to the MOSFET structure, where the deep implants at source and drain are different. However the channel source and drain extension implants are equal as in a MOSFET. This BSC-FET is representative for a device with a very shallow source implant. The impact of this structure regarding general device behaviour and consequences for circuit design is objective to this investigation.

Implementation into 130nm, 90nm, 65nm standard processes are presented and compared. The BSC-FET offers better short channel effects like reduction of Drain Induced Barrier Lowering (DIBL). The output conductance is lower compared to CMOS which is especially interesting for analog applications. In some applications the integrated substrate contact can be of advantage, as it can reduce total chip area up to 3%. Due to the inherent substrate contact of the BSC-FET a tripple well process is needed for stacked devices.

HL 35.8 Thu 12:00 H13

Acoustically driven integrated Mach-Zehnder-Interferometer
— Markus Beck[1], Mauricio de Lima[2], Rudolf Hey[1], and •Paulo Santos[1] — [1]Paul–Drude–Institut für Festkörperelktronik, Hausvogteiplatz 5-7, D-10117 Berlin, Germany — [2]Materials Science Institute, University of Valencia, P. O. Box 22085, E-46071 Valencia, Spain

We demonstrate a compact modulator based on conventional ridge waveguides (WGs) monolithically fabricated on GaAs. The modulator consists of a Mach-Zehnder interferometer (MZI) driven by a surface acoustic wave (SAW) in the GHz range, which modulates the refractive index in the two arms of the interferometer. The effect on the interference is maximized by choosing the spatial separation between the arms to be an odd multiple of the acoustic wavelength λ_{SAW} in order to modulate the arms with opposite phases. The modulated waveguide length is minimized by using a focusing interdigital transducer to generate a narrow and intense acoustic beam. Peak-to-peak modulation exceeding 90% of the average transmission is demonstrated with a modulated waveguide length of approximately 15 μm, which is significantly shorter than for comparable approaches.

HL 35.9 Thu 12:15 H13

Beitrag abgesagt — •XXX XXX —

HL 35.10 Thu 12:30 H13

Gated Hallbars and Pseuod MOSFETs for mobility measurements on biaxially tenisle strained silicon on insulator layers
— •Sebastian Frederik Feste[1], Joachim Knoch[2], and Siegfried Mantl[1] — [1]Forschungszentrum Jülich, Institut für Bio- und Nanosysteme 1 (IBN 1-IT), Deutschland — [2]IBM Rüschlikon, Zürich, Schweiz

We studied the mobility enhancement in biaxially tensile strained silicon on insulator (SSOI) layers with gated Hallbar MOSFETs and Pseudo-MOSFETs with Schottky contacts. The SSOI was fabricated by layer transfer of a strained-Si/SiGe virtual substrate to an oxidized wafer. The final structure was obtained by wet etching of the remaining SiGe. Hall measurements allow a measurement of the carrier concentration and mobility. The advantage of this method is the direct measurement of the inversion layer carrier concentration so that no assumption about the gate capacitance is necessary. Psi-MOSFETs allow one to preform transistor-like measurements on SOI wafers without the need for actual device processing. They can therefore be used as a quick-turnaround tool for SOI wafer characterization. The dependence of the extracted mobility on the Schottky barrier height and the channel length has been studied and compared to the values obtained form the gated Hallbars. Both techniques show a nearly doubled electron mobility of 580cm^2/Vs for SSOI of different thicknesses compared to SOI.