DF 4: High-k dielectrics for highly scaled Silicon-based Micro- and Nanoelectronics

Time: Monday 14:00–17:00 Location: EB 107

Invited Talk DF 4.1 Mon 14:00 EB 107

High-k gate dielectrics on silicon and on high-mobility semiconductors: Atomic-scale phenomena underlying transistor performance — •Martin M. Frank — IBM T.J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY 10598, USA

Computer chip technology is undergoing a materials revolution: Hafnium-based high-permittivity ('high-k') dielectrics are replacing the silicon oxide gate insulator in metal-oxide-semiconductor field-effect transistors (MOSFETs); and metals are replacing the polycrystalline silicon gate electrode. These changes allow us to extend the exponential increase in integration density and performance known as Moore's Law. Researchers are even attempting to replace the silicon channel itself by high-carrier-mobility semiconductors, such as germanium, III-V compounds, carbon nanotubes, or graphene.

I will provide an overview of the materials science underlying MOSFET performance. First, properties and scaling of the traditional silicon oxide insulator will be summarized. Then, focus will be on non-epitaxial Hf-, Al-, and Ti-based dielectrics on silicon and on high-mobility semiconductors. We describe how processing parameters determine stack structure, e.g. continuity of the high-k layer, interface composition, and oxygen vacancy concentration. Comparing Si to Ge and III-V substrates, differences in interface formation will be rationalized based on thermodynamic considerations. Finally, we illustrate how the stack structure determines device characteristics such as gate leakage, gate stack capacitance, threshold voltage, and carrier mobility.

Invited Talk DF 4.2 Mon 14:40 EB 107

Molecular Beam Epitaxy of crystalline oxides on Si for C-MOS and for the monolithic integration of semiconductors on Silicon — •Saint-Girons Guillaume[1], Merckling Clément[1], El-Kazzi Mario[1], Becerra Loic[1], Regreny Philippe[1], Patriarche Gilles[2], Largeau Ludovic[2], Favre-Nicolin Vincent[3], and Hollinger Guy[1] — [1]INL/UMR5270-Site ECL, 36 av Guy de Collongue, 69134 Ecully cedex, France — [2]LPN UPR20/CNRS Route de Nozay, 91460 Marcoussis cedex — [3]cCEA/DRFMC/SP2M, 17 rue des Martyrs 38054 Grenoble and UJF, BP53, 38041 Grenoble cedex 9, France

In this contribution, a detailed description of the growth mechanisms and structural properties of high-k Al_2O_3, Gd_2O_3 and amorphous $LaAlO_3$ on Si will be presented. On the basis of these studies, relevant oxide/Si systems will be proposed that fulfill the requirements of future C-MOS systems. In particular, very promising electrical characteristics have been obtained showing that the (amorphous $LaAlO_3$)/Si system is compatible with ITRS recommendations in terms of EOT and leakage current. Moreover, it will also be shown that InP/oxide heterointerfaces present a quasi-ideal compliant behavior that opens the way to the monolithic integration of III-V heterostructures on Si for advanced micro and optoelectronic applications.

Invited Talk DF 4.3 Mon 15:05 EB 107

Damascene metal gate technology: A solution to high-k gate stack challenges? — •Udo Schwalke — Darmstadt University of Technology, Darmstadt, Germany

Since the late 1960s, the normal fabrication method of CMOS transistors is known as the "gate first" approach. As the name indicates, gate dielectric and gate electrode are made first, i.e. prior to the self-aligned formation of the source (S) and drain (D) junctions by ion-implantation. As long as the gate stack has been made out of polycrystalline silicon and silicon dioxide, process integration was not an issue. Both materials are able to withstand high annealing temperatures and are compatible with reactive ion etching. However, after introducing novel gate stack materials, like high-k gate dielectrics and metal gate electrodes, the situation has been changed completely. These new materials are sensitive and degrade during high-temperature processing. In order to circumvent process-induced gate-stack damage, we have developed a "gate last" process flow, in which the self-aligned gate stack is made after S/D junctions. For the first time, fully functional metal gate MOSFETs with crystalline high-k dielectric have been fabricated by means of chemical mechanical polishing (CMP). Electrical results and details of the "gentle" damascene metal gate technology will be presented. To which extent the "gate last" approach is a general solution to the high-k metal gate challenges will be discussed.

Invited Talk DF 4.4 Mon 15:30 EB 107

Do new materials solve the upcoming challenges of future DRAM memory cells? — •Uwe Schröder — Qimonda Dresden GmbH & Co. OHG, Koengisbruecker Strasse 180, 01099 Dresden

A permanent trend in miniaturization of semiconductor DRAM devices has required continuous introduction of new materials. Specially, for capacitor and transistor applications a strong push for new dielectric materials and metal electrodes is ongoing. As design rules for capacitors are dropping below 50nm geometrical options turn out to be more and more challenging. Dielectrics with permittivity values more than 30 and metal electrodes become important. In the past few years the introduction of AlO-, HfO-, and ZrO-based dielectric materials with TiN electrodes were reported. The main focus of this work is to compare mixed and laminate dielectric films in terms of crystallographic phase resulting in capacitance enhancement and leakage current improvement. Optimized dielectric properties were reached for doped HfO- and ZrO dielectrics in a cubic/ tetragonal phase. Simultaneously, conventional SiON/Poly-Si gate devices will be replaced by high-k dielectric/metal gate structures for continuous scaling. Here industry narrowed down the choice of high-k dielectrics to HfO-based materials. Depending on the device specifications different metal electrodes are proposed. Trends, progress, and challenges will be reviewed.

Invited Talk DF 4.5 Mon 16:10 EB 107

AVD and ALD developments for next generation MIM capacitors and memory applications — Peter K. Baumann, Christoph Lohe, and •Michael Heuken — AIXTRON AG, Aachen, Germany

Atomic layer deposition (ALD) enables deposition of electrode, dielectric and barrier layers on high aspect ratio trench structures and has been widely used. However, due to its nature the throughput is typically limited. Atomic vapor deposition (AVD®) is a special type of metal organic vapor deposition (MOCVD) that enables deposition with high precursor gas phase saturation. This results in improved throughput while maintaining conformal deposition on moderate aspect ratio trench structures. Based on the International Roadmap for Semiconductors (ITRS) for front end, for DRAM at the 50nm and below technology node metal-insulator-metal (MIM) structures will be required [1]. Also conformal step coverage on structures with aspect ratios of 1:60 and higher as well as an equivalent oxide thickness (EOT) of less than 1nm will be necessary. Other memory applications (e.g. phase change memory) require less advanced aspect ratios, opening possibilities for AVD®. ALD and AVD® have been used to deposit electrode and dielectric films based on e.g. TiN, Ru, TaSiN as well as HfO_2, ZrO_2, Al_2O_3. Results for the different deposition techniques and various process conditions will be presented and compared considering use for memory applications.

[1] Front end, International Roadmap for Semiconductors (Semiconductor Industry Association, Palo Alto 2006 update).

Invited Talk DF 4.6 Mon 16:35 EB 107

MIM Capacitors for Wireless Communication Technologies — •Christian Wenger — IHP, Im Technologiepark 25, 15236 Frankfurt Oder

The high-k Metal-Insulator-Metal (MIM) capacitor BEOL integration into circuits for wireless communication is characterized by the efforts toward increasing the capacitance density, reducing the leakage current density and improving the voltage linearity. In particular, the achievement of sufficient capacitance voltage linearity in high-k MIM capacitors is still a challenge. Based on fundamental physical effects, the origin of the quadratic voltage dependence of high-k MIM capacitors will be presented.