DS 27: Trends in Ion Beam Technology: From the Fundamentals to the Application

Time: Thursday 14:30–16:00 Location: H 2013

Invited Talk DS 27.1 Thu 14:30 H 2013

Surface engineering with ion beams: from self-organzied nanostructures to ultra-smooth surfaces — •Frank Frost, Bashkim Ziberi, Axel Schindler, and Bernd Rauschenbach — Leibniz-Institut für Oberflächenmodifizierung e. V.

Low-energy ion beam sputtering, i. e. the removal of atoms from a surface due to the impact of energetic ions or atoms, is an inherent part of numerous surface processing techniques. Besides the actual removal of material, this surface erosion process often results in a pronounced alteration of the surface topography. Due to different roughening and smoothing mechanisms a multitude of topographies can result from surface erosion. Under certain conditions, sputtering results in the formation of well ordered patterns. This self-organized pattern formation is related to a surface instability between curvature dependent sputtering that roughens the surface and smoothing by different surface relaxation mechanisms. If the evolution of surface topography is dominated by relaxation mechanisms surface smoothing can occur.

In this presentation the current status of self-organized pattern formation and surface smoothing by low-energy ion beam erosion is summarized. In detail it will be shown that a multitude of patterns as well as ultra smooth surfaces can develop, particularly on Si surfaces. Additionally the most important experimental parameters that control these processes and theoretical approaches describing the surface topography evolution are discussed. Finally, examples are given for the application of low-energy ion beams as a novel approach for passive optical device engineering for many advanced optical applications.

Invited Talk DS 27.2 Thu 15:00 H 2013

Rare earth doping of GaN — •André Vantomme — Instituut voor Kern- en Stralingsfysica and INPAC, K.U.Leuven, Celestijnenlaan 200 D, B-3001 Leuven, Belgium

Group III-nitrides, e.g. GaN, are suitable hosts for incorporating rare earths (RE), potentially resulting in visible light emission at various wavelengths. Ion implantation is commonly employed for semiconductor doping, presenting several advantages over other techniques, such as in situ doping. However, implantation induces radiation damage to the lattice, which can have detrimental effects on the electrical and optical properties of the material. Further, the exact lattice site of the implanted ions has to be known, since it strongly influences the intensity and splitting of the optical transitions. We have studied the defect accumulation during RE (Er, Eu, Tm) implantation into GaN, as well as the lattice site of the implanted ions, varying a range of experimental parameters such as the implanted fluence, temperature, angle of the beam incidence, energy, annealing conditions The defect concentration and profile were assessed by channelling spectroscopy and high-resolution X-ray diffraction. By emission channelling, the lattice site of implanted radioactive ions was accurately determined, including the root mean square displacement from the ideal sites. From our study, we derived a general model correlating the induced defects, strain and the ion lattice sites, irrespective of the implantation parameters. Finally, these structural properties were linked to the optical and electrical characteristics of the nitride, investigated by photo- and cathodoluminescence and by deep level transient spectroscopy respectively.

Invited Talk DS 27.3 Thu 15:30 H 2013

Junction and Channel Engineering for Advanced Microprocessors — •Manfred Horstmann — AMD Saxony LLC & Co. KG, Wilschdorfer Landstraße 101, 01109 Dresden, Germany

An overview of state of the art Silicon on Insulator CMOS transistors used for 65 nm/45 nm volume manufacturing of multicore microprocessors will be given. AMDs unique technology and transistor progression model as well as the key challenges to increase the performance per watt of microprocessor products will be described. For advanced SOI transistors stress engineering has become a standard feature since the 90 nm technology node due to gate oxide scaling limitations [1]. Especially techniques which induce local strain such as compressive and tensile stressed over-layer films, embedded-SiGe, and stress memorization, are key to enhance transistor and product performance [2]. To reduce the lateral and vertical device dimensions advanced (Laser or Flash) annealing in combination with low energy implants has been applied [3]. These anneal processes yield an improved dopant activation for active and gate regions resulting in lower source-drain resistance and gate depletion without any additional diffusion. Starting with the 45nm node, reducing parametric scattering for instance by improving tilt, twist, energy etc. control of implant steps are an emerging topic for performance optimization. A novel technique to statistically investigate parametric scattering, directly in the microprocessor chip, will be presented.

[1] M. Horstmann, et al., IEDM 2005, p. 243 [2] A. Wei et al., VLSI 2007 [3] Th.Feudel et al., RTP Conference, Kyoto, 2006