HK 47: Instrumentation und Anwendungen II

Zeit: Freitag 14:00–15:45 Raum: 2D

HK 47.1 Fr 14:00 2D

Integration and Commissioning of the ALICE TRD Global Tracking Unit — •Jan de Cuveland for the ALICE-TRD-Collaboration — Kirchhoff-Institut für Physik, Universität Heidelberg

The Transition Radiation Detector (TRD) is one of the main detectors of the ALICE experiment at the LHC. One of its primary objectives is to trigger on high momentum electrons and jets.

The trigger concept requires fast event reconstruction involving complex computations. Based on data from 1.2 million analog channels, the reconstruction must be performed within 6 μs to contribute to the Level-1 trigger decision. A dedicated hardware architecture achieves the processing in the required time by means of massive parallelism.

Optical multi-gigabit links with a total bandwidth of 2.7 TBit/s transfer pre-processed track segment data from the detector front-end electronics to the Global Tracking Unit (GTU). The GTU reconstructs tracks from up to 20 000 track segments, calculates particle momenta based on track curvatures and finally makes the trigger decision. In case of a Level-1 accept, compressed analog data is shipped to the GTU and buffered for transmission to the data acquisition system.

The GTU consists of 109 dedicated CompactPCI boards based on Xilinx Virtex-4 FX FPGAs. The complete system has been built and installed at the LHC. This presentation focuses on the commissioning of the ALICE TRD GTU system. It also summarizes results from the latest test at the CERN PS beam and from ALICE cosmics runs.

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HK 47.2 Fr 14:15 2D

The new Data Acquisition system of the HADES experiment. — •Marek Palka for the HADES-Collaboration — Jagiellonian University, Cracow, Poland — Gesellschaft für Schwerionenforschung, Darmstadt, Germany

The main goal of the HADES DAQ upgrade project is to achieve a primary data acquisition rate of 20 kHz also for events with maximum charged particle multiplicity (i.e Au+Au collisions). We favor a modular design to increase the scope of applications (e.g. to integrate new detector systems) and simplify the debugging. A first version (TRBv1) of a system fullfiling the above requirements was recently used during the production runs to read out four detector subsystems. However, in order to work at the highest rates and provide fast pre-processing for the different trigger levels, an improved board was necessary (TRBv2). Such a board has been built, featuring a fast optical link (2.5Gb/s), Tiger-Shark DSP (600 MHz), 2 Gb SDRAM and ETRAX-FS multiprocessor. In this talk, the real-world performance of this upgraded TRB will be presented. To this board customized Add-On boards are plugged providing the connectivity and functionality necessary to interface the different detector systems used in HADES. Following the same concept, an optical Hub with 16 transceivers (32 Gb/s) and the Central Trigger System have been implemented as Add-On boards. We will present the current status of all these different components and describe how they interact in a complete system.

HK 47.3 Fr 14:30 2D

The readout concept of the PANDA Micro-Vertex-Detector — •Tobias Stockmanns, Fabian Hügging, Marius C. Mertens, Andrey Sokolov, and James Ritman for the PANDA-Collaboration — FZ Jülich GmbH, Institut für Kernphysik I, Jülich

The "AntiProton ANnihilations at DArmstadt" - experiment, PANDA, is one of the main experiments of the "Facility for Antiproton and Ion Research" (FAIR) which replaces and extends the existing GSI-facility at Darmstadt. Primary physics goals include precision spectroscopy of charmonium states, establishment of gluonic excitations, the study of modifications of meson properties in the nuclear medium, and precision gamma-ray spectroscopy of single and double hypernuclei. For many of these physics goals an identification of D-mesons via the detection of a secondary vertex is essential. Therefore, a special micro vertex detector (MVD) is foreseen which allows precise tracking of all charged particles.

One of the major challenges in the development of the MVD is the triggerless readout concept of the PANDA experiment. This requires that all detected hit points in the MVD have to be transmitted to the DAQ-system in the control room without any pre selection and with a minimum of material. The maximum data rate is in the order of 100 Gbit/s. To achieve this goal a readout concept was developed which will be presented in this talk.

HK 47.4 Fr 14:45 2D

A multipurpose programmable read-out chip — •Massimiliano De Gaspari, Hans-Kristian Soltveit, and Johanna Stachel — Physikalisches Institut, Heidelberg

A mixed-signal integrated chip in IBM 130nm technology suitable to a variety of detectors with different requirements is under development. The CBM experiment at FAIR could be a good candidate for the use of this chip.

The chip can read out 128 channels, which can be masked in groups of 16, 32 or 64. The multichannel ASIC includes a low noise PreAmplifier and Shaping Amplifier (PASA), a Peak Detector (PD), a Time-to-Amplitude Converter (TAC) and fast arbitration and sequencing logic to concentrate the data before it is sent to a pipelined Analog-to-Digital Converter (ADC).

The chip is self-triggered, which is essential for applications where the detector pulses arrive randomly in time.

The PASA is programmable for different detector capacitances (from 1pF to 50pF), input pulse polarity, preamplifier gain, peaking time (from 20 to 200ns) and conversion gain in order to suit a wide range of application requirements.

The ADC is programmable to support either 8, 10 or 12 bit resolution with a conversion rate from 1MHz to 100MHz; the switched-capacitor bias network provides bias currents proportional to the operating frequency.

Simulations of the ADC will be shown together with plots of the expected performance.

HK 47.5 Fr 15:00 2D

n-XYTER on a Prototype Front End Board for CBM — •Rafal Lalik and Christian Schmidt for the CBM-Collaboration — Gesellschaft fuer Schwerionenforschung mbH, Plankstrasse 1, 64291

The CBM experiment of FAIR does state considerable development challenges in the wide fields of detector technology, front-end electronics, FPGA based data acquisition as well as data compression logic. On various elements of this readout chain, first development efforts have started.

The n-XYTER ASIC chip is a modern readout system to work with particle detectors. It will here be employed as a first prototype for the dedicated readout ASIC to be developed for FAIR. High integration and small size comprise a big challenge for the PCB designer. Placing the chip, routing fan-in connections with very thin tracks and simultaneously caring about controlled impedances and input capacitances require from the designer to employ PCB-technology on its cutting edge. A prototype front-end board for the n-XYTER ASIC intended for the broad application in CBM detector prototyping will be presented.

HK 47.6 Fr 15:15 2D

Production and test of FEE components for ALICE TRD — •Venelin Angelov for the ALICE-TRD-Collaboration — KIP, Im Neuenheimer Feld 227, 69120 Heidelberg

The Transition Radiation Detector for ALICE at the LHC contains 540 drift chambers and over 1.2 million analog channels. The readout electronics is based on two specially developed chips. The TRAP chip performs analog-to-digital conversion (ADC), digital filtering, preprocessing, quad-CPU based tracking and data shipping over a data tree. The whole detector contains 65,000 such chips, packed as Multi-Chip-Modules (MCM) together with the analog preamplifier-shaper chip. We give an overview of the production of the TRAP chips and of the MCM modules, as well as their automated testing.

The output of the readout data tree is feed to an Optical Readout Interface board (ORI), 1080 in the whole detector. This board is based on commercially available components and works at 2.5Gbps. The production is finished, all boards are configured for operation. We give short report about the test results.

HK 47.7 Fr 15:30 2D

The Upgrade of the Multiwire Drift Chambers readout in the HADES experiment at GSI. — •Attilio Tarantola[1,4],

Burkhard Kolb[2], Christian Müntz[1], Marek Palka[3], Herbert Ströbele[1], Joachim Stroth[1], and Michael Traxler[2] for the HADES-Collaboration — [1]Institut fuer Kernphysik, J. W. Goethe-Universitaet Frankfurt, Germany — [2]GSI, Darmstadt, Germany. — [3]Jagiellonian University, Krakow, Poland. — [4]Helmholtz Research School, Frankfurt. Work supported by BMBF, GSI, EU.

One of the main goals of the HADES upgrade project is the realization of a new data acquisition scheme for the 24 Multiwire Drift Chambers (MDCs), which allows to increase the readout speeds. The general concept of the upgrade is based on the TDC Readout Board (TRB), which will be the common readout platform for all HADES detectors. It has two very high data-rate digital interface connectors for integrating Add-On boards. The MDC Add-On board is the interface to the detector Front End Electronic (FEE). It provides resources to configure the FEE and allows to readout the digital data generated by the FEE. The MDC Add-On, together with the TRB, replaces the existing readout electronics. It communicates with the chamber FEE through parallel bus cables. The MDC Add-On configures and reads out the Time to Digital Converters (TDCs) which are accommodated on FEE boards mounted on the chamber's frames. In a second stage of the upgrade we shall replace the parallel bus with serial optical links, while keeping all DAQ functionalities already achieved in the first stage with the MDC Add-On.