HK 5: Instrumentation und Anwendungen II

Zeit: Montag 14:00–16:00 Raum: 2D

Gruppenbericht HK 5.1 Mo 14:00 2D

ATCA Compliant Compute Nodes for HADES, PANDA and BESIII — •Tiago Perez[1], Camilla Gilardi[1], Xu Hao[2], Daniel Kirschner[1], Igor Konorov[4], Andreas Kopp[1], Kris Korcyl[5], Wolfgang Kühn[1], Johannes Lang[1], Jens Sören Lange[1], Ming Liu[1], Zhen'An Liu[2], Alexander Mann[4], Da Peng[2], Johannes Roskoss[1], Lars Schmitt[3], and Shuo Yang[1] for the HADES-Collaboration — [1]II. Physikalisches Institut, Univ. Giessen — [2]IHEP Beijing — [3]GSI Darmstadt — [4]TU München — [5]Jagiellonian University Krakow

FPGA based compute nodes with multi-Gbit/s bandwidth capability using the ATCA architecture are designed to handle tasks such as event building, feature extraction and high level trigger processing. Each board is equipped with 5 Virtex4 FX60 FPGAs. A single module supports an aggregate bandwidth of 30 GB/s featuring 8 optical links which are connected to RocketIO ports. Furthermore, four Gbit Ethernet links are available for easy connectivity to the PC world. A single ATCA crate can host up to 14 boards which are interconnected via a full mesh backplane. The system will be used to implement the trigger upgrade of the HADES and BESIII detector systems and will serve as a prototype platform for PANDA DAQ and triggering. The system is scalable and can be optimized for pipelined and parallel architectures. This work is supported in part by BMBF(6GI-179/6GI-180), BMBF-WTZ and GSI

HK 5.2 Mo 14:30 2D

Konstruktion und Implementierung eines hochauflösenden Transientenrekorders — •Florian Herrmann, Jochen Barwind, Horst Fischer, Fritz-Herbert Heinsius, Donghee Kang, Wolfgang Käfer, Kay Königsmann, Louis Lauser, Kambiz Mahboubi, Andreas Mutter, Frank Nerling, Christian Schill, Sebastian Schopferer, Anselm Vossen, Markus Webel, Konrad Wenzl und Heiner Wollny für die COMPASS-Kollaboration — Physikalisches Institut der Albert-Ludwigs-Universität Freiburg

Für physikalische Experimente mit hohen Raten erfordern Signalpulse mit Längen von 40ns, schnellen Anstiegsflanken und großen dynamischen Bereichen Transientenrekorder mit sehr hohen Abtastraten. Zusätzlich können, wie bei vielen Spektroskopieexperimenten und z.B. dem COMPASS Rückstossdetektor, Doppelpulse entstehen, die durch den Transientenrekorder erfasst und mit mathematischen Hilfsmitteln separiert werden sollen, um Zeit und Amplitude der Signale gewinnen zu können. Weiterhin sollen diese Informationen direkt zu einer Triggererzeugung verwendet werden.

Für die Bewerkstelligung dieser Aufgaben wurde ein Transientenrekorder mit 12bit und 1 Gsps Abtastrate entwickelt. Kombiniert mit erweiterten Speicherkapazitäten stellt dieses Modul nicht nur ein totzeitfreies Auslesesystem mit hoher Triggerverzögerung dar, sondern genügt durch den mit DSP Elementen bestückten FPGA den numerischen Herausforderungen für Doppelpulsseparation und Zeitauflösungen im Subnanosekundenbereich. Dieses Projekt wird vom BMBF unterstützt.

HK 5.3 Mo 14:45 2D

Intelligent Platform Management Controller (IPMC) for ATCA Compute Nodes * — •Johannes Lang — II. Physikalisches Institut JLU Giessen for the HADES, BESIII and PANDA collaboration

Future experiments like PANDA will create a large amount of data which has to be processed online. For this purpose a high performance FPGA based Compute Node is being developed in Giessen. This device, compatible with the ATCA standard (Advanced Telecommunication Computing Architecture), will be used for the upgrade of the BESIII and HADES DAQ systems as well as for the data acquisition and trigger of the PANDA experiment.

ATCA specifications require a slow control manager (IPMC) for every ATCA compliant device. Our realization consists of a microcontroller based add on card procuring shelf communication via I2C. It manages power negotiation & airflow and monitors voltages, status & component temperatures. A connection to the front panel allows to display basic information and to directly execute tasks like reset, hot swap or initialization of certain boot modes. The implementation of the IPMC will be presented.

* Work supported in part by: BMBF 06 Gi 180 & 179, GSI

HK 5.4 Mo 15:00 2D

Entwicklung von TDC ASICs an der GSI — •Holger Flemming und Harald Deppe für die CBM-Kollaboration — Gesellschaft für Schwerionenforschung, Darmstadt

Für den Flugzeitdetektor des CBM-Experimentes wird eine Ausleseelektronik benötigt, die hohen Anforderungen in Bezug auf Zeit- und Doppelpulsauflösung genügt und sich in das Konzept der Triggerlosen Datenerfassung einfügt. Dazu wird zur Zeit an der GSI ein TDC ASIC entwickelt, der eine Zeitauflösung $\sigma_\tau < 25$ ps aufweist und bei einer durchschnittlichen Rate $r \approx 100$ kHz Pulse im Abstand von $\tau \leq 3,5$ ns trennen kann.

Nachdem als Konverterkern sowohl ein Zeit- Amplitudenwandler, als auch ein DLL basierter TDC auf ihre Eignung hin untersucht wurden, wird zur Zeit an einem ersten TDC Prototypen gearbeitet, mit dem Systemtests durchgeführt werden können.

Im Vortrag werden zunächst die Funktionsprinzipien der beiden untersuchten Konverterkerne beschrieben, die Messergebnisse der untersuchten Testchips präsentiert und dann das Konzept des geplanten TDCs erläutert.

HK 5.5 Mo 15:15 2D

A Data Acquisition Backbone Core library. — Jörn Adamczewski, •Hans G. Essel, Nikolaus Kurz, and Sergey Linev — GSI, Darmstadt, Germany

For the new experiments at FAIR new concepts of data acquisition systems have to be developed like the distribution of self-triggered, time stamped data streams over high performance networks for event building. The Data Acquisition Backbone Core (DABC) is a general purpose software framework designed for the implementation of such data acquisition systems. It provides the event building over networks like InfiniBand or Gigabit Ethernet. All kinds of data channels (front-end systems) are supported by program plug-ins into functional components of DABC like data input, combiner, scheduler, event builder, analysis and storage components. Commands and parameters of DABC and its application plug-ins are published by DIM servers. A Java based Graphical User Interface provides the dynamic control and visualization of these components. Application specific GUIs can be added. After a testing phase, DABC can be used to develop high performance data acquisition systems. Besides that DABC will be used for the implementation of various test beds needed for the final design of data acquisition systems at FAIR like detector tests, readout components test, and data flow investigations. The development of key components is supported by the FutureDAQ project of the European Union (FP6 I3HP JRA1).

HK 5.6 Mo 15:30 2D

High performance data acquisition with InfiniBand. — Jörn Adamczewski, •Hans G. Essel, Nikolaus Kurz, and Sergey Linev — GSI, Darmstadt, Germany

For the new experiments at FAIR new concepts of data acquisition systems have to be developed like the distribution of self-triggered, time stamped data streams over high performance networks for event building. In this concept any data filtering is done behind the network. Therefore the network must achieve up to 1 GByte/s bi-directional data transfer per node. Detailed simulations have been done to optimize scheduling mechanisms for such event building networks. For real performance tests InfiniBand has been chosen as one of the fastest available network technology. The measurements of network event building have been performed on different Linux clusters from four to over hundred nodes. Several InfiniBand libraries have been tested like uDAPL, Verbs, or MPI. The tests have been integrated in the Data Acquisition Backbone Core software DABC, a general purpose data acquisition library. Detailed results will be presented. In the worst cases (over hundred nodes) 50% of the required bandwidth can be already achieved. It seems possible to improve these results by further investigations. The development of key components is supported by the FutureDAQ project of the European Union (FP6 I3HP JRA1).

HK 5.7 Mo 15:45 2D

Design and implementation of a hierarchical DAQ network — •Norbert Abel[1], Frank Lemke[2], and Wenxue Gao[2] for the CBM-Collaboration — [1]KIP Heidelberg — [2]University of Mannheim

The FAIR project comes with many new challenges. One of them is the data acquisition (DAQ) - the handling of the huge data streams produced by the detectors. DAQ can be partitioned into three major parts. Firstly, the different analog signals produced by one detector have to be digitalized and filtered. Secondly, the preprocessed data of several detectors has to be combined. And thirdly, the combined data has to be analyzed and stored. We are in a design process of such a three step DAQ for the STS (Silicon Tracker System). In our actual setup the first step is done by the so called FEE (Front End Electronic) containing the nXYTER, an ADC and the ROC (Read Out Controller). The nXYTER-Board is measuring the value and the exact time of a signal peak. This data has to be synchronized and the data not representing a signal peak has to be filtered out by the ROC. The FEE has multiple ways to pass the data. In our first test setup we did implement the Ethernet protocol, directly connecting the FEE with a PC running analyzing software. In future the FEE will be connected via optical fiber to Data Combiner Boards (DCB) and Active Buffer Boards (ABB) realizing the second step. The DCB with its multiple MGT's concentrates the data and presents a inner node of a hierarchical buildup. The ABB represents the data buffer and receiver for a root node. It is connected to a PC (via PCI Express), which is responsible for the third step.