HK 53: Accelerators and Instrumentation II

Time: Wednesday 14:00–16:00 Location: H-ZO 90

HK 53.1 We 14:00 H-ZO 90

Trigger Schemes of the ALICE TRD Global Tracking Unit — •Felix Rettig — Kirchhoff Institute for Physics, University of Heidelberg

The Transition Radiation Detector of the ALICE experiment is designed to provide a fast Level-1 trigger for different classes of signatures as well as full event information for offline reconstruction.
A total of 1.2 million analog channels is processed massively parallel in a two-stage approach to derive a trigger decision within 6 μs after the interaction. Pattern matching algorithms are employed in 65 000 FEE Multi-Chip Modules to parametrize up to 20 000 stiff track segments. The detector data is then transferred to the second stage, the Global Tracking Unit (GTU), via 1 080 optical fibres at an aggregate bandwidth of 2.7 TBit/s.
The GTU itself consists of 109 dedicated FPGA-based processing nodes forming a three-level hierachy. 90 Track Matching Units perform online 3D track reconstruction and momentum calculation within 1.2μs. Full track and momentum information of azimutal detector segments is then forwarded to one of the 18 Supermodule Units for trigger pre-computation. The top-level Trigger Generation Unit finally computes the overall TRD trigger decision.
This talk focuses on the current status of the GTU and the GTU-based cosmic trigger used for ALICE data taking and supermodule production during 2008. Developments for future trigger schemes in p-p operation, especially for specific decays (J/ψ, Y) involving online invariant-mass calculations as well as for jets, will be presented.

HK 53.2 We 14:15 H-ZO 90

Dynamic system management for the Alice HLT using the SysMES framework — •Timo Breitner and Camilo Lara for the ALICE-HLT-Collaboration — Kirchhoff Institut für Physik, Universität Heidelberg

The task of the ALICE High Level Trigger (HLT) is to reduce incoming detector data from 25 GB/s to at most 1.25 GB/s. This can be achieved by selecting, compressing and filtering the event data in a parallel pipelined chain of analysis processes. The data flow framework used for this purpose supports dynamic runtime reconfiguration of the analysis hierarchy.

System Management in the HLT is performed by the SysMES framework which manages both the computing infrastructure as well as the HLT analysis application. It is able to automatically reconfigure the chain of analysis processes with the following three techniques:

- Monitoring of the infrastructure and application components together with the most critical resources.
- Correlating the monitored values to detect local or global errors
- Execution of actions to return the application into a stable and correct state, in particular to avoid the loss of data. This includes moving, adding and removing processes as needed.

The first version of the HLT application management includes monitors for 18 critical resources and the possibility to react to failures by dynamically reconfiguring the HLT application. Future steps include the development of new more sophisticated rules based on experiences to be gained during the experiment's commissioning phases.

HK 53.3 We 14:30 H-ZO 90

An FPGA based preprocessor for the ALICE HLT — •Torsten Alt and Volker Lindenstruth for the ALICE-HLT-Collaboration — Kirchhoff Institute of Physics, University of Heidelberg, Germany

With more than 550.000 channels the Time Projection Chamber is the main tracking detector in ALICE. Particles traversing the TPC will create a track of primary ionized electrons which drift towards the read-out pads in the endcaps where they create a charge cloud which is then digitized. To achiev a better spatial resolution than the pad size this charge cluster is spread over several pads. In order to reconstruct the particle trajectories the center of gravity of the clusters needs to be calculated before this information is passed to the tracking algorithms. In the ALICE High-Level-Trigger (HLT) this clusterfinding is done by an FPGA preprocessor. Raw data is received directly from the detector via optical links, unpacked and feed into the Fast-Cluster-Finder (FCF) processing unit which calculates the centers of gravity. The results are then transfered into the main memory of the HLT. The FCF algorithm has been optimized to take advantage of the FPGA resources allowing parallel processing of the data and pipelining resulting in a design speed of more than 150 MHz. First results with simulated data show that the 216 FCF processors in the HLT are able to process an event with about 7200 charged particles in less than 1 millisecond.

HK 53.4 We 14:45 H-ZO 90

Analog FEE for High Counting Rate Transition Radiation Detector — •Vasile Catanescu, Daniel Bartos, and Gheorghe Caragheorgheopol — National Institute for Physics and Nuclear Engineering, Bucharest, Romania

The first version of a front-end electronics (FEE) based on Application Specific Integrated Circuit (ASIC) for high counting rate transition radiation detectors developed at NIHAM-NIPNE for CBM experiment at FAIR will be presented. The new front-end electronics consists of eight analog channels for TRD signals processing. The ASIC is designed in CMOS 0.35 microns AMS technology. Each channel has two analog outputs, one fast output with a semi-Gaussian signal useful for fast sampling ADCs and a second output with a peak sens information. The mother board contains some level translators and buffers for interface with standard acquisition system. This front-end electronics could easily fit with other high counting rate experiments.

HK 53.5 We 15:00 H-ZO 90

FairRoot — Florian Uhlig and •Mohammad Al-Turany — GSI Darmstadt

FairRoot is a simulation, reconstruction and analysis framework developed at the GSI in Darmstadt for the upcoming FAIR experiments. Currently it is used by the CBM and Panda collaborations.

To achieve the flexibility to use different transport models (currently support for Geant3, Geant4 and Fluka) and different event generators (e.g. UrQMD, Pluto) FairRoot is based on Root and Virtual Monte Carlo. %to use already existing %and well tested software. The complete simulation/analysis process is steered using Root macros, which for example define the detector layout or the transport model. FairRoot uses the Root executable and loads during runtime all needed libraries for the simulation/analysis on the fly. FairRoot deliver also a generic event display based on ROOT and a generic track propagator based on the Geane code.

To provide Makefiles for many Linux flavors, Mac OS X and Solaris CMake is used to generate native Makefiles for the different platforms. To get a fast and comprehensive overview, the project is build on all of the supported platforms automatically on different clients. The produced results are send to a server for display.

HK 53.6 We 15:15 H-ZO 90

Intelligent Platform Management Controller (IPMC) for ATCA Compute Nodes * — •Johannes Lang[1], Ming Liu[1], Zhen'An Liu[2], Qiang Wang[2], Hao Xu[2], and Wolfgang Kühn[1] for the PANDA-Collaboration — [1]II. Physikalisches Institut, JLU Giessen — [2]Institute for High Energy Physics, Beijing

The PANDA experiment with its high data rate presents a significant challenge for the trigger and data acquisition system. Therefore a main building block of the data processing concept, the Compute Node, has been designed and is currently being tested. It will also be used for the upgrade of the HADES trigger system and comprises 5 FPGAs and high bandwidth connections (RocketIO, Gigabit Ethernet) taking advantage of a new shelf standard originating from the telecommunication sector (the Advanced Telecommunication Computing Architecture (ATCA)). This standard requires each supported module to feature a dedicated control unit, the IPMC.

An implementation of such a controller, a micro-controller utilizing add-on card will be presented. It can be plugged into the Compute Node and communicates with a shelf manager via the I2C bus. Applications include negotiation of power levels, reading of sensor data for temperature, voltages and current. In addition, status and configuration of the FPGAs on the Compute Node can be checked and changed. First experience with a prototype board will be reported.

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HK 53.7 We 15:30 H-ZO 90

Dynamical Partial Reconfiguration for Data Acquisition — •Norbert Abel, Jano Gebelein, and Udo Kebschull for the CBM-Collaboration — KIP Heidelberg

Xilinx FPGAs like Virtex2, Virtex4 or Virtex5 provide the possibility to be reconfigured partially and dynamically. This means, that parts of the hardware can be exchanged while the rest of the circuit is running untouched. Nowadays, typical applications of dynamical partial reconfiguration (DPR) are streaming, low power, reconfigurable coprocessors and fault tolerance. Furthermore, DPR can help to increase design flexibility and scalability while the design itself becomes smaller at the same time. Regarding to the DAQ (data acquisition) in high energy physic experiments, all these topics are of interest. Unfortunately, today it is still very complex to use DPR, since the developer has to understand the reconfiguration techniques in detail to be able to use DPR. That causes a small usage of DPR in DAQ systems, yet. In the following we want to present a DPR framework that makes it possible to use the complete DPR techniques without going in detail with the underlying technology. Thus, our framework enables regular DAQ developers to use all the advantages coming with partial reconfiguration.

HK 53.8 We 15:45 H-ZO 90

Fault-tolerant Logics for FPGA Linux — •Jano Gebelein, Norbert Abel, and Udo Kebschull for the CBM-Collaboration — Kirchhoff-Institute for Physics, University of Heidelberg

The increasing use of SRAM-based reconfigurable architectures at important areas of research and development (like particle accelerators and space applications) brings new, currently partially unattended effects on top. An already well known, but nevertheless important problem of such systems is its susceptibility to radiation which increases in conjunction with particle flux and energy. Regarding to current knowledge, errors induced by Single Event Upsets (SEU) and Single Event Transients (SET) are handled exclusively in hardware by the use of spacial and temporal redundancy features. Our field of research is to extend conventional fault tolerance to multiple layers of embedded computer systems, starting with the FPGA bit layer and ending up in the software application layer to get a maximum of radiation tolerance in systems running FPGA Linux in radiation susceptible environments. Only a collaboration of all these layers is able to create an adequate amount of data security and process integrity.