Continuous downsizing of field effect transistors is about to reach physical limits and calls for new device concepts. The Tunnel FET (TFET), based on a gated pin-diode, is a promising candidate for future CMOS technology due to its superior properties like small sub-threshold slope, fabrication without sophisticated technology, and good temperature stability. However, increasing the on-current remains challenging. We propose to use thick ultra-high-k materials as gate dielectrics in order to induce a higher electric field at the tunnelling junction due to the well-known fringing field effect. While worsening the device characteristics of a conventional MOSFET, it turns out that this effect significantly enhances the device performance of TFET devices. The reason is that the off-current is given by a pin-diode leakage current, while the on-current increases exponentially with the electric field. On-currents fulfilling the actual ITRS roadmap and slopes down to 20 mV/dec are observed in simulations of the device by using a generic diode with k = 200 and d = 102 nm. As aggressive downsizing of the device is not needed, the usability for high-frequency applications is very good due to the low gate capacitance.

Separation and Analysis of different leakage mechanisms in modern MOSFETs — Guntrade Rolli, Matthias Goldbach, Andre Wachowiak, Juergen Holz, and Lothar Frey

CMOS device development via gate length reduction is driven by the requirement for performance enhancement under power consumption control. Gate length scaling is enabled by reducing gate oxide thickness, parasitic capacitances as well as source/drain junction depth. These actions typically lead to increasing device leakage currents. I will present detailed investigations of leakage currents and mechanisms on industry fabricated PFET devices with channel length smaller than 100 nm. The influence of the gate induced drain leakage (GIDL), drain induced barrier lowering (DIBL), p+n-junction leakage and gate leakage on the total device current loss is studied with temperature dependent current-voltage and capacitance-voltage measurements. Two types of sample systems have been investigated:

- PFETs with ultra shallow source/drain (carbon co-implantation)
- PFETs with high-k gate dielectric and metal gate

The analysis reveals the relative magnitude of the different leakage current contributions, the DIBL effect and GIDL control the leakage for increasing drain bias. The underlying mechanisms (direct tunneling, defect assisted etc.) are investigated.

Vertical IMOS with n-doped deltas for high temperature applications — Tina Kubot, Ulrich Arellin, Peter Iskra, Torsten Sulima, and Ignaz Eisele

The demands for process control in high temperature (HT) environments like engines or exhaust systems grow e.g. due to stricter requirements in CO2-emission. The low temperature tolerance of common silicon based devices becomes a great issue in the development of suitable sensors and readout electronics. Increased intrinsic charge carrier density and decreased p-n-junction barrier height can reduce the device performance down to total failure of the devices.

With the IMOS we have introduced a device concept which has proven its suitability for HT-environments. After realizing p-delta planar doped barrier (PDB) FET structures with superior Drain-Source leakage currents and high On-Off-Ratios at 500 K we now present n-doped PDB-structures. We show investigations on the temperature dependent barrier properties of highly phosphorus doped deltas in p++-i-n++-i-p++-diode structures fabricated by molecular beam epitaxy. The deltas have a thickness of 3 nm and a doping level of >10^{19} cm^{-3}. Temperature dependent I-V-measurements were carried out from room temperature up to 500 K. For the measurements a semiconductor parameter analyzer with a heated chuck was used. The electrical characteristics of these test devices show a good barrier formation by the delta layer even at elevated temperatures.
First prototype of a novel memory device based on self-organized quantum dots — •Andreas Marent¹, Tobias Nowozin², Martin Geller², Johannes Gelze², and Dieter Bimberg¹ — ¹Institut für Festkörperphysik, TU Berlin, Hardenbergstr. 36, 10623 Berlin — ²Fachbereich Physik und CeNIDE, Universität Duisburg-Essen, Lotharstrasse 1, 47048 Duisburg

We have developed a memory concept (QD-Flash) based on self-organized quantum dots (QDs) [1] with the potential to overcome the restrictions of nowadays most important semiconductor memory, the Flash-memory. The main disadvantage of the Flash-memory results from the use of Si/SiO₂ which leads to a fundamental trade-off between write time and storage time. In contrast, using III-V semiconductors in the QD-Flash, ultra fast write times (< ns) in combination with a long storage time (>> 10 years) can be realized.

We demonstrate a first prototype of the QD-Flash with full functionality using InAs-QDs in Al₀.₉Ga₀.₁As as memory units. The performance of the prototype has been evaluated up to room temperature. Read out of the stored information was successfully realized by measuring the resistance of a two dimensional hole gas formed in a GaAs/Al₀.₉Ga₀.₁As quantum well embedded below the QD-layer.