HL 26: Focused Session: Novel nanowires electronic device concepts

Time: Wednesday 9:30–13:00 Location: HSZ 01

Topical Talk HL 26.1 Wed 9:30 HSZ 01

Nanoelectronics - Why 1D nanowires? — •Joerg Appenzeller — School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, USA

While nano-materials have been explored extensively for the last fifteen years or so, the societal impact has been rather limited due to the lack of a substantial amount of nano-applications. This is in part a result of the time it takes to gain the necessary understanding of the material properties and underlying physics/chemistry, to a larger extend it is due to the fact that most studies do not cover materials and devices aspects with a clear application in mind simultaneously. For example, nano-materials frequently are discussed in the context of high density electronic applications. This seems to be a natural choice due to their intrinsic smallness. However, nano-materials have to offer unique electronic properties that enable new types of devices applications in order to be suitable for a future nano-electronics. One of the * if not THE - most pressing questions in the area of electronics is how to reduce power consumption. Here we discuss the impact of dimensionality and body thickness - the diameter in case of a nanowire - on the performance of nano-devices. We will elucidate on the impact of the wire diameter on the device on-state and off-state as well as the scaling of wire based transistors and the implications for low power device applications.

Topical Talk HL 26.2 Wed 10:00 HSZ 01

Doping limits in silicon nanowires — •Mikael Björk, Heinz Schmid, Joachim Knoch, Heike Riel, and Walter Riess — IBM Research GmbH, Ruschlikon, Switzerland

The operation of electronic devices relies heavily on the density of free charge carriers available in the semiconductor, a quantity that is usually well controlled by the addition of dopant atoms. The fabrication of ultimately scaled semiconductor devices will thus depend significantly on the ability to precisely control the location and number of active impurity atoms in the host semiconductor. As dimensions are scaled down the presence of interfaces and materials adjacent to the semiconductor become more important and can eventually completely determine the electronic properties of the device. Here we experimentally demonstrate the in-situ doping limits of silicon nanowires and that the free carrier density in nanoscale semiconductor wires is size dependent due to a reduction in the amount of ionized impurities. By measuring the electrical conduction of doped silicon nanowires as a function of wire radius, temperature and dielectric surrounding we present experimental proof of a deactivation of the doping atoms in the wires, which is due to a dielectric mismatch between the nanowire core and the surrounding.

15 min. break

Topical Talk HL 26.3 Wed 10:45 HSZ 01

Polarity control of silicon nanowire transistors by electrostatic coupling to the Schottky contacts — Walter Michael Weber[1,2], Lutz Geelhaar[4], Franz Kreupl[3], Henning Riechert[4], and •Paolo Lugli[2] — [1]Namlab gGmbH, Dresden, Germany — [2]TU - Munich, Institute for Nanoelectronics, Munich, Germany — [3]Qimonda AG, Neubiberg, Germany — [4]Paul Drude Institute, Berlin, Germany

One of the challenges for implementing nanoscale semiconductors in future electronics is the accurate adjustment of the charge carrier concentration. We present an innovative method of creating p- and n-type FETs by employing intrinsic Si nanowires (NW) as the active region. This method does not require doping, but takes advantage of the inherent NW geometry and simply relies on the electrostatic control of the bands near the source- and drain- (S/D) contacts. The FETs are built from longitudinal $NiSi_2$/Si/$NiSi_2$ NW-heterostructures. The intruded metallic $NiSi_2$ segments act as S/D -regions and introduce a Schottky barrier (SB) at their interface to the Si active region. Temperature activation measurements were used to reveal the relation between the applied electric fields and the charge carrier injection over the contacts. Accordingly, the transistor's conductance was electrostatically steered by switching between thermionic emission and thermal assisted tunneling. This effect was employed to provide additional functionality to the transistors. By independently coupling each Schottky contact through separate top gates the device polarity could be controlled. This simple method enables the possibility to conceive complementary logic circuits without the use of doping.

Topical Talk HL 26.4 Wed 11:15 HSZ 01

Antimonide-based nanowire devices — •Lars-Erik Wernersson — Lund University, Sweden

III/V nanowires are attractive for implementation in various transistor configurations. For instance, InAs nanowire FETs have shown high transconductance and good subthreshold characteristics at 50 nm Lg [1]. Capacitance studies of the III/V MOS structure confirmed the transistor operation and provided values for the interface state density [2]. Also heterostruture barriers have been introduced to the channel to shift Vt [3].

The introduction of Antimon-based materials into the channel enables new functionalities for the nanowire transistors. GaSb nanowires have demonstrated good p-type conduction [4], while InSb nanowires allow the introduction of a very high mobility material [5]. Besides, InSb has a very large g-factor.

In this talk, the performance for short-channel InAs nanowire transistors and MOS capacitors will be discussed. Furthermore, experimental data for growth and electrical performance of GaSb and InSb nanowires will be presented and discussed.

[1] Thelander, et al IEEE Electron Device Lett 29, 206 (2008) [2] Roddaro, et al, Appl. Phys. Lett. 92, 253509 (2008); [3] Lind, et al Nano Lett., 6 (9), 1842 (2006) [4] Jeppsson, et al Journal of Crystal Growth23, 5119 (2008) [5] Caroff et al, Small 4, 878 (2008)

15 min. break

Topical Talk HL 26.5 Wed 12:00 HSZ 01

Rf-characterization of III-V-Nanowire FET: Problems and Results — •Franz Tegude and Werner Prost — Univ. Duisburg-Essen

Nanowire fieldeffect transistors (NW-FET) are a straight forward continuation of downscaling in microelectronics. Further, because of their excellent transport properties, III-V-semiconductor materials have demonstrated record high frequency potential. This contribution addresses mainly, but not exclusively, InAs-n-channel MISFET prepared by a bottom-up approach employing the vapor-liquid-solid (VLS) epitaxial growth mode. Single NWs are processed yielding gate lengths in the micrometer and sub-micrometer range. Due to the nanometer scale two aspects become core problems with respect to FET device performance and characterisa-tion: parasitics, and mismatch to nearly exclusively used 50 Ohm rf measurement environment. Corner frequencies of about 15 GHz are presented, together with deembedding techniques to yield intrinsic and parasitic device parameters. In addition, rf characteristics are used for transport data evaluation, because standard methods like Hall characterisation is not immediately applicable to nanowire geometry.

Topical Talk HL 26.6 Wed 12:30 HSZ 01

Semiconductor nanowires as building blocks for quantum devices — •Thomas Schäpers[1], Sergio Estevez Hernandez[1], Gunnar Petersen[1], Robert Frielinghaus[1], Shima Alagha[1], Christian Blömers[1], Thomas Richter[1], Raffaella Calarco[1], Hans Lüth[1], Michel Marso[1], and Michael Indlekofer[2] — [1]Institute of Bio- and Nanosystems (IBN-1), JARA-Fundamentals of Future Information Technologies, Research Centre Jülich, 52425 Jülich, Germany — [2]Informationstechnologie and Elektrotechnik, Wiesbaden University of Applied Sciences, Am Brückweg 26, 65428 Rüsselsheim, Germany

Semiconductor nanowires are versatile building blocks for the design of future electronic devices. Among the many possible materials, InN is particularly interesting because of its low energy band gap and its high surface conductivity. At low temperatures electron interference effects often play an important role in the transport characteristics of nanostructures. We studied the electronic transport of InN nanowires grown by plasma-assisted molecular beam epitaxy. The wires had a diameter ranging from 40 nm to 130 nm and a length of approximately 1 μm. Information on the phase-coherent transport was gained from the measurement of universal conductance fluctuations. It was found that at low temperatures phase-coherence is maintained in the complete wire structure, which is an important prerequisite for quantum devices. For

nanowires comprising a very small diameter of approximately 40 nm pronounced flux-periodic oscillations in the magneto-conductance were observed. This effect is attributed to the formation of coherent circular quantum states on in the tube-like surface electron gas.