HK 48: Instrumentierung VIII

Zeit: Donnerstag 14:00–15:45 Raum: HG VIII

HK 48.1 Do 14:00 HG VIII

The GSI Event-Driven TDC with 4 Channels GET4 — •Harald Deppe and Holger Flemming for the CBM-Collaboration — GSI Helmholtzzentrum für Schwerionenforschung GmbH, Experiment Elektronik ASIC-Design, Darmstadt, Germany

The GSI Event-driven TDC GET4 is the first prototype of a high resolution low power event driven TDC for the CBM-Time of Flight detector readout. The design specifications according to the CBM-ToF requirements are a very high time resolution of better than 25 ps and a double hit resolution of less than 5 ns. The TDC has to cope with an event rate of up to 100 kHz per channel. The time core architecture is based on a Delay Lock Loop followed by a clock driven hit register. For the event handling derandomistion units adapted from FiFo's are implemented and the readout is controlled by a token ring structure. The serialized data transmission could cover different event types like data, error or synchronisation events. The ASIC was submitted in October 2008 and is presently under test at GSI Darmstadt.

HK 48.2 Do 14:15 HG VIII

Radiation Studies on the UMC 180 nm CMOS Process at GSI — •Sven Löchner, Harald Deppe, and Holger Flemming for the CBM-Collaboration — GSI Helmholtzzentrum für Schwerionenforschung GmbH, Experiment Elektronik ASIC-Design, Darmstadt, GERMANY

Radiation damages to electronic components are an important issue for the future experiments at the new Facility for Antiproton and Ion Research (FAIR). One of the preferred technologies of the CBM collaboration for ASIC developments is the 180 nm UMC CMOS process. In this regard the ASIC design group of the GSI Experiment Electronic department has been launched a research project, including the development of an ASIC called GRISU. The main goal is the characterisation of Single Event Effects (SEE) and Total Ionising Dose effects (TID) on the 180 nm UMC process as well as the installation of different testing sites for heavy ion irradiation at the GSI linear accelerator.

Within the talk a short overview of the GRISU test ASIC is given. Thereafter the different SEE testing possibilities for ASIC chips with the GSI heavy ions accelerator are briefly outlined. Finally some test results for SEE measurements as well as TID degradation and annealing are reported.

HK 48.3 Do 14:30 HG VIII

Integrierte Auslese - Elektronik für das CALICE Hadron - Kalorimeter — •Sandra Christen für die CALICE-Germany-Kollaboration — Deutsches Elektronen Synchrotron DESY Hamburg

Ein neuer Prototyp eines hochgranularen Hadronen Kalorimeters mit analogem Read-Out (AHCAL) für den **I**nternational **L**inear **C**ollider (ILC) Detektor wird z. Z. von der CALICE Kollaboration gebaut und getestet. Das angestrebte Ziel ist eine Jet-Energie Aufösung von $30\%/E_{Jet}$. Damit wird das Particle Flow (PFLOW) Konzept validierbar bei dem jedes Teilchen eines Jets identifiziert und seine Energie im jeweils bestauflösenden Detektor nachgewiesen wird. Das CALICE HCAL für den ILC bei $90 - 1$ TeV Schwerpunktsystem basiert daher auf Plastik Szintillator Kacheln von $3 \times 3 \times 0{,}3$ cm^3, und neuartigen Silizium Photomultipliern (SiPM).

Die Daten - Aquisition (DAQ) wird durch ASIC Chips der Generation SPIROC 2 gesteuert. Diese besitzen je 36 Kanäle mit 12-bit TDC und ADC Daten pro Kanal bei einer Speichertiefe von 16 für 16 mögliche ILC Events pro Bunch-Crossing. Desweiteren steuern die ASICs die Bias-Vorspannungen der 36 SiPMs sowie die Shaping Time und Koppelkondensator-Kapazitäten für die Aussteuerung der dynamischen Bandbreite der ADCs. Der Prototyp der 2. Generation wird etwa 2500 Kanäle besitzen. Diese 2 x 6 **H**CAL **B**ase **U**nits (HBUs) mit je 144 Detektorkanälen werden für Machbarkeitsstudien am Teststrahl vorbereitet.

HK 48.4 Do 14:45 HG VIII

The Pretrigger System for the ALICE Transition Radiation Detector — •Jörg Lehnert[1], Jochen Klein[2], Tobias Krawutschke[3], Ken Oyama[2], Rainer Schicker[2], and Stefan Schmiederer[2] for the ALICE-TRD-Collaboration — [1]Institut für Kernphysik, Goethe-Universität Frankfurt — [2]Physikalisches Institut, Universität Heidelberg — [3]Fachhochschule Köln

The Transition Radiation Detector (TRD) of the ALICE experiment at the CERN Large Hadron Collider (LHC) provides electron identification and tracking in the central barrel as well as fast triggering (6μs). The frontend electronics (FEE) consisting of 75000 multichip modules has a total power consumption of less than 65kW by keeping the digital electronics in a low power mode after processing an event. A fast wakeup signal for the FEE within 400ns after an interaction is needed to capture the TRD drift signals over the full time range and to ensure a low latency of data processing.

A dedicated hardware system provides this so-called pretrigger signal based on the direct analog or digital signals from the fast ALICE subdetectors TOF, V0 and T0 or the LHC bunch counter. Specific hardware components are mounted inside the L3 magnet close to the respective detectors to minimize signal propagation delays. Pretrigger algorithms employing conditions on multiplicities and geometrical coincidences are implemented in field programmable gate arrays.

We will describe the setup of the pretrigger system and report on its performance during operation of the ALICE TRD in pp collisions since Nov. 2009. This work is supported by BMBF and GSI.

HK 48.5 Do 15:00 HG VIII

Digitalisierung und Echtzeitanalyse von Detektorsignalen mit GANDALF — •Louis Lauser, Stefan Bartknecht, Horst Fischer, Florian Herrmann, Kay Königsmann, Christian Schill, Sebastian Schopferer und Heiner Wollny für die COMPASS-Kollaboration — Physikalisches Institut der Albert-Ludwigs-Universität Freiburg

Zur Identifikation von Rückstoß-Protonen aus exklusiven Streuprozessen werden am COMPASS-Experiment die Flugzeit von Teilchen sowie ihr spezifischer Energieverlust im Rückstoß-Proton-Detektor (RPD) gemessen. Zur Verarbeitung der Pulse und Weiterleitung der Daten wird das GANDALF-System eingesetzt, dessen Virtex-5 FPGA Architektur eine schnelle Echtzeitanalyse der Daten selbst bei hohen Raten erlaubt. Die Weiterleitung der Daten an die Massenspeicher erfolgt wahlweise über S-Link, Ethernet oder USB. Über eine VME64x-Schnittstelle kann das Modul konfiguriert und überwacht werden. Die VXS-Backplane erlaubt einen Datenaustausch mit einem dedizierten Triggermodul von bis zu 18 GB/s.

Eine universelle Verwendung des GANDALF-Systems ist mit auf Steckkarten angeordneten Eingängen gewährleistet. Als Transientenrekorder wird GANDALF zusammen mit Analog-Mezzanine-Karten betrieben. Mit 12-bit ADCs und einer Abtastrate von bis zu 1 GHz werden die Signale totzeitfrei digitalisiert und sowohl Integral als auch Zeitpunkt des Signals berechnet. Weiterhin ist das GANDALF-System als Scaler- und TDC-Einheit mit jeweils 128 Kanälen einsetzbar. Dieses Projekt wird vom BMBF unterstützt.

HK 48.6 Do 15:15 HG VIII

Design and Implementation of the Read-Out-Controller for the GET4 chips — •Sebastian Manz and Udo Kebschull for the CBM-Collaboration — KIP Universität Heidelberg

The ToF detector of the CBM experiment will assemble about 15000 GET4 ASICs, all clocked from the same 156.25MHz source. Those chips create a very precise timestamp from detected hits and deliver the data via a serial LVDS link to the ROC. At the moment, one ROC interfaces up to 28 GET4 chips.

For the readout of all those chips, several tasks need to be performed. One has to combine the data from different chips in one datastream, sort the data in epochs, eventually perform simple compression algorithms on the data, and finally send them over a communication interface to the DAQ-Cluster. A further challenge is to synchronize the so gathered data with the data from other detectors.

The ROC also needs to provide a control interface to the GET4 chips and to the ROC itself. Commands can be send over the communication interface to the ROC. For certain tasks it is useful or even necessary to execute multiple commands in a very short time frame. For this purpose short command lists can be send together in one packet to the ROC. For longer command lists and lists that need to be executed more often the ROC provides a programmable list of commands stored on the FPGA.

This presentation gives an overview of the design of the ROC's GET4-readout module and present some data that has been taken in a test setup.

HK 48.7 Do 15:30 HG VIII

A demonstrator for the CBM Time Of Flight wall electronic readout chain — •Pierre-Alain Loizeau[1], Norbert Herrmann[1], Mircea Ciobanu[2], Harald Deppe[2], Holger Flemming[2], Jochen Frühauf[2], Karsten Koch[2], Serguey Linev[2], Sebastian Manz[3], and Walter F.J. Müller[2] for the CBM-Collaboration — [1]Physikalisches Institut, Universität Heidelberg, Heidelberg, Germany — [2]GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany — [3]Kirchhoff-Institut für Physik, Universität Heidelberg, Germany

The Compressed Baryonic Matter (CBM) experiment at FAIR requires a time resolution better than 80ps for its Time of Flight (ToF) wall in order to achieve the particle identification goals necessary to perform its physics program.

This implies a 40ps limit in the total electronic resolution. Following the concept of the CBM detector readout, the timing system has to operate in self-triggered mode, where each hit receives a time stamp. The demonstrator consists of a high bandwidth preamplifier discriminator, an event-driven TDC, clock generation and distribution system, a dedicated Readout Controller and an optical readout interface. To allow the usage of existing systems as reference, the demonstrator includes synchronization mechanisms with triggered systems. The scheme is kept strictly differential to suppress common mode sensitivity.

The concept of the demonstrator and first results obtained with the CBM software environment will be presented.

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