DF 6: Focus Session: High-k and high mobility materials for CMOS

Time: Tuesday 10:00–13:10 Location: H11

Invited Talk DF 6.1 Tue 10:00 H11

Gate Oxides beyond SiO_2 and the High K Materials Revolution — •Darrell Schlom — Department of Materials Science and Engineering, Cornell University, USA

A major materials milestone has been achieved that transforms the materials makeup of silicon-based field-effect transistors: the SiO_2 gate dielectric has been replaced by a hafnium-based dielectric in microprocessors produced by leading manufacturers. The incredible electronic properties of the SiO_2/silicon interface are the reason that silicon has dominated the semiconductor industry and helped it grow to over 250 billion US dollars in annual sales. The shrinkage of transistor dimensions has led to tremendous improvements in circuit speed and computer performance. At the same time, however, it has also led to exponential growth in the static power consumption of transistors due to quantum mechanical tunneling through an ever-thinner SiO_2 gate dielectric. This spurred an intensive effort to find an alternative to SiO_2 with a higher dielectric constant (K) to temper this exploding power consumption and enable Moore's law to continue. In this talk the comprehensive materials analysis to identify silicon-compatible materials that go beyond SiO_2 (i.e., with higher K and sufficient bandgap) will be described, together with how these materials have enabled improvements in MOSFETs, DRAM, and emerging semiconductor devices.

5 min. break

Topical Talk DF 6.2 Tue 10:45 H11

Advanced CMOS transistor technologies using HKMG and strained Silicon for high performance applications — •Manfred Horstmann — Globalfoundries Dresden

In this paper we present an overview about CMOS transistor technologies for advanced circuit applications. To achieve a *high performance per watt* figure of merit, transistor technology elements like strained Si, aggressive junction scaling and high K metal gate technology need hand-in-hand development with multiple core- and power efficient designs. These techniques have been developed, applied and optimized for 45nm volume manufacturing and are currently in ramp for the 28 & 32nm "Foundry" technology nodes at GLOBALFOUNDRIES in Dresden. Different High K metal gate integration schemes and their advantages for different circuit applications will be discussed. An outlook on 22nm technology will be given.

Topical Talk DF 6.3 Tue 11:10 H11

Amorphous ternary high-k oxides on Si and higher mobility substrates — •Marcelo Lopes[1,2], Eylem Durgun-Ozben[1,2], Alexander Nichau[1,2], Roman Luptak[1,2], Martin Roeckerath[1,2], Juergen Schubert[1,2], and Siegfried Mantl[1,2] — [1]Institute for Bio- and Nanosystems (IBN1), Research Center Juelich, Juelich, Germany — [2]JARA-Fundamentals of Future Information Technologies, Juelich, Germany

The miniaturization of metal-oxide-semiconductor field effect transistors (MOSFETs) is approaching fundamental limits. Novel materials are needed in order to continue the CMOS scaling. High-k dielectrics combined with semiconductors with better transport properties than Si is an attractive alternative. Strained Si (sSi), Ge, and SiGe are candidates with intrinsic higher carrier mobilities than Si. However, one of the issues that still remains is the challenge to achieve a high quality interface between the high-k film and these semiconductor substrates. The search for alternative high-k oxides that could offer stable interfaces offering a low density of electrically active defects has become a topic of major interest. Ternary rare earth oxides such as the scandates ($LaScO_3$, $GdScO_3$ or $DyScO_3$) and $LaLuO_3$ have been identified as promising high-k candidates for Si-based CMOS applications. In this contribution, we will review our results on the structural and electrical properties of $REScO_3$ (RE = La, Gd, Tb, Sm) and $LaLuO_3$ amorphous thin films deposited on Si. In addition, the integration of these oxides with high mobility substrates such as sSi, Ge, and SiGe will be presented.

Invited Talk DF 6.4 Tue 11:35 H11

Aspect Ratio Trapping: A Heterointegration Solution for Ge and III-V CMOS — •James Fiorenza — AmberWave Systems, Salem, NH, USA

Enhanced MOSFETs using high mobility non-silicon channel materials are being intensively investigated for future CMOS nodes. This research path is extremely promising, but significant challenges remain. Perhaps the largest challenge is the heterointegration of the high mobility materials with silicon. A heterointegration technique called Aspect Ratio Trapping (ART) is well suited to the unique integration requirements of mobility-enhanced CMOS. This technique involves epitaxial growth in narrow (< 500 nm), high aspect ratio silicon dioxide trenches. Threading dislocations generated by the lattice mismatch between the epitaxial material and silicon are trapped by the sidewalls of the trenches, greatly reducing the surface dislocation density. This technique been shown to be effective with a variety of relevant cubic semiconductors including Ge, InP and GaAs. The resulting buffer layers can be thinner than 500 nm, more than an order of magnitude thinner than traditional graded buffer heterointegration approaches, a critical advantage for CMOS applications.

5 min. break

Topical Talk DF 6.5 Tue 12:20 H11

Wafer Bonding Techniques for Advanced CMOS — •Manfred Reiche — Max-Planck-Institut für Mikrostrukturphysik, Halle

There are numerous discussions on future strategies of complementary metal-oxide-semiconductor (CMOS) device scaling. According to simulations, the gate length of an ultimately scaled MOSFET is well below 10 nm. Devices with gate lengths as small as 10 nm were already demonstrated using existing technologies. Apart from scaling new materials are employed to boost the transistor performance. Besides new materials for gate stacks (high-k materials, metal gates), interconnects, etc., new substrates are strongly required. For instance, silicon-on-insulator (SOI) is one of the most important substrates for high performance applications. The combination of the advantages of SOI with high-mobility channel materials (strained silicon, germanium) offers additional possibilities to improve the device performance. All these substrates are realized by wafer bonding techniques. The different wafer bonding techniques and their fundamental physical and chemical principles as well as the application to advanced CMOS substrates are reviewed.

Topical Talk DF 6.6 Tue 12:45 H11

Si wafer engineering: single crystalline oxides as buffers for the integration of alternative semiconductors — •Alessandro Giussani[1], Peter Zaumseil[1], Olaf Seifarth[1], Markus Andreas Schubert[1], Peter Storck[2], and Thomas Schroeder[1] — [1]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany — [2]SILTRONIC AG, Hanns-Seidel-Platz 4, 81737 Muenchen, Germany

Single crystalline oxides are the object of intensive research as buffers for the integration of functional semiconductors on the mature Si platform. The interest is motivated on the one hand by the demand for cheap semiconductor substrates (i.e. Ge & GaN) on Si, and on the other hand by CMOS semiconductor (i.e Si & Ge)-on-insulator technologies. The main advantage of the oxide templates is the high flexibility to tune important epitaxy parameters of the overgrowing semiconductor. Bixbyite-based heterostructures are used by our group for Si, Ge and GaN integration. In the talk, special attention will be dedicated to solid solutions of (Pr2O3)1-x(Y2O3)x (x = 0-1) heterostructures which can be used for the growth of lattice-matched and -mismatched SiGe systems. As an example, pure Ge thin film heterostructures on cubic Pr2O3 are demonstrated. The grown Ge epilayers are single crystalline, atomically smooth and free of impurities from the buffer and Si. Moreover, a complex characterization of the Ge epilayer defect structure is presented by a combination of XRD and TEM.