

HL 10: Devices II

Time: Monday 14:00–15:45

Location: H13

HL 10.1 Mon 14:00 H13

Ballistic rectification in an asymmetric Si/SiGe cross junction with modulated electron density — •DANIEL SALLOCH¹, ULRICH WIESER¹, ULRICH KUNZE¹, and THOMAS HACKBARTH² — ¹Werkstoffe und Nanoelektronik, Ruhr-Universität Bochum, D-44780 Bochum — ²DaimlerCrysler Forschungszentrum Ulm, D-89081 Ulm

We demonstrate a substantial efficiency increase in an injection-type ballistic rectifier due to a modulated electron density in its active region. The rectifier is a nanoscale four-terminal Ψ -shaped cross junction [1] fabricated from a high-mobility Si/SiGe heterostructure. Two nanoscale Schottky gates are locally deposited on top of the central stem above and below the cross junction. In addition to the inertial-ballistic rectified voltage, which will develop between the upper and lower end of the central stem if a current is injected between the branches [1], a hot-electron thermopower voltage [2] establishes across the saddle-point potential formed below the local gate for negative gate-voltages [3]. At $T = 4.2$ K we observe an increase of the rectified signal due to the superposed hot-electron thermopower for negative gate voltages. Depending on the position of the constriction in the stem, a sign reversal of the output signal is also demonstrated. Both signals are experimentally separated in a modified device geometry.

[1] M. Knop *et al.*, Appl. Phys. Lett. **88**, 082110 (2006)

[2] L. W. Molenkamp *et al.*, Phys. Rev. Lett. **65**, 1052 (1990)

[3] D. Salloch *et al.*, Appl. Phys. Lett. **94**, 203503 (2009)

HL 10.2 Mon 14:15 H13

Dot-Field Effect Transistor: Using locally strained silicon for MOSFET applications — •JÜRGEN MOERS¹, JULIAN GERHARZ¹, GREGOR MUSSLER¹, CLEBER BIASOTTO², VLADIMIR JOVANOVIĆ², LIS NANVER², and DETLEV GRÜTZMACHER¹ — ¹Institute for Bio and Nanosystems, Research Centre Jülich, D-52425 Jülich, Germany — ²DIMES, TU Delft, Mekelweg 4, 2628 CD Delft, The Netherlands

Typical dimensions of electronic devices have been scaled into the sub-50nm range. The use of strained silicon for carrier mobility enhancement is a route to meet the challenges occurring at those dimensions. By means of templated self assembly of SiGe-dots on prepatterned substrates and epitaxial overgrowth a silicon layer is created, which is strained on top of the SiGe-dots and their near vicinity. Integrating the MOSFET on the dot will use the strain to improve the device performance.

During processing special emphasis has to be laid on the overlay accuracy and low thermal budget processing to prevent intermixing of the strained silicon layer with the SiGe-dot. While the gate dielectric was deposited by CVD the activation of dopants was done by laser annealing.

DotFET devices with gate lengths between 50 and 200 nm and gate widths between 100 and 300 nm were fabricated with 15 nm SiO₂ as gate dielectric. First measurements show an improved current drivability in respect to reference devices processed on the same wafer, indicating the suitability of this device concept. Further improvements can be reached by removing the SiGe-dot from beneath the gate.

HL 10.3 Mon 14:30 H13

Ammonium hydroxide (NH₄OH) as etch-stop chemical for highly boron-doped silicon δ -layers — •OLIVER HAMMER, FLORIAN PALITSCHKA, HELMUT LOCHNER, TINA KUBOT, DOROTA KULAGA-EGGER, DANIEL BECKMEIER, CAROLIN AXT, JOSEF BIBA, RONNY SCHINDLER, MARC DRESSLER, TORSTEN SULIMA, and WALTER HANSCH — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

The downscaling process in current microelectronics results in smaller devices and thinner layers. A proper etch-stop for such thin layers, e.g. boron-doped δ -layer (<10nm) in a vertical device, becomes more and more challenging. Therefore an etchant with an exceedingly high selectivity to boron-doped silicon is needed. Only two wet-chemical silicon etchants, TMAH and the not common NH₄OH, are capable for CMOS technology and are not too highly toxic. The major advantage of NH₄OH in comparison to TMAH is its high selectivity of 1:8000 for intrinsic silicon with respect to boron-doped silicon. The disadvantages are formation of hillocks and more pronounced surface roughness compared to TMAH. We optimize etching parameters by

variation of the etch temperature, the concentration of NH₄OH in water and the ratio of 2-propanol in the solution to achieve an etch-stop at a δ -layer without breaking it. Recent experiments show that a solution of TMAH and 2-propanol decreases the surface roughness and the formation of hillocks. Due to this we also perform tests with 2-propanol in a NH₄OH solution. Finally we etch a bulk unipolar device (BUD) to determine the electrical characteristics of the exposed δ -layer.

HL 10.4 Mon 14:45 H13

Interface Defect Study by GIDL Current and Charge Pumping Measurements on MOSFET Devices — •GUNTARDE ROLL¹, STEFAN JAKSCHIK¹, ANDRE WACHOWIAK², MATTHIAS GOLDBACH², and LOTHAR FREY³ — ¹Namlab gGmbH, D-01187 Dresden — ²Qimonda, D- 01099 Dresden — ³Fraunhofer IISB, D-91058 Erlangen

The continued improvement in CMOS technology requires the scaling of transistor dimensions while maintaining acceptable leakage currents. One key to performance enhancement is a good process control of the gate oxide to silicon interface properties, such as a low defect density and reduced oxide regrowth. The Gate Induced Drain leakage (GIDL) enhances power consumption when the gate is turned off. The GIDL current increases as the interface oxide thickness is reduced, due to electric field increase. Another factor which varies the GIDL leakage is the interface trap density at the gate edge.

We report the investigation of two types of samples. First the dependence of the interface traps on the carbon content in the ultra shallow Source/Drain junction of PFETs is evaluated using a lateral profiling Charge Pumping technique. The electrical measurements reveal an increase of GIDL current by carbon co-implantation.

In the second set of samples the spacer material and the gate etch parameters of devices with high-k dielectric are varied. This reduces the interface oxide regrowth and decreases the GIDL current. We present a correlation between GIDL current and Charge Pumping measurements and compare both the influence of the electric field and the interface trap density on the leakage.

HL 10.5 Mon 15:00 H13

Application of a parameter extraction method for MOSFETs — •JOSEF BIBA, DOROTA KULAGA-EGGER, TORSTEN SULIMA, and WALTER HANSCH — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

For statistical process control in industrial production of semiconductors it is important to obtain MOSFET parameters, which are not directly accessible. An effective but merely known method to determine the effective channel length and the channel resistance is the one of Kazuo Terada and Hiroki Muta. Here the output characteristics of transistors with same channel width but various channel lengths are used. This approach showed good results in simulations and with processed self-aligned poly-silicon-gate MOSFETs.

We present an investigation of the application of this method on metal-gate transistors, where the gate stack is aligned by lithography. This results in an asymmetric underdiffusion of the gate. For the investigation n-channel MOSFETs were produced using Spin-On-Dopant (SOD) technology for Source/Drain doping. The effective channel length and the channel resistance were determined using Terada Muta and compared to SIMS and contact resistant measurements.

HL 10.6 Mon 15:15 H13

Electrical characterization of doped semiconductor nanostructures with Scanning Microwave Microscopy — •MATTHIAS A. FENNER¹, HASSAN TANBAKUCHI¹, STEPHAN STREIT², CHRISTINE BAUMGART², MANFRED HELM², and HEIDEMARIE SCHMIDT² — ¹Agilent Technologies, Campus Kronberg, 61476 Kronberg, Germany — ²Institute of Ion Beam Physics and Materials Research, Forschungszentrum Dresden-Rossendorf e.V., P.O. Box 510119, 01314 Dresden, Germany

Highly sensitive scanning microwave microscopy (SMM) with a capacitance resolution in the aF range [1] has been used to investigate the electrical properties of doped semiconductor nanostructures in the microwave frequency range from 1.5 GHz to 6 GHz at different dc offset biases. The microwave signal S₁₁ reflected by the sample is related to the impedance of the sample. Superimposing an ac voltage in the kHz

range one also gains information about the derivative of the S11 signal (dC/dV), which is dependent on the doping density in the semiconductor, circuit resistance, and reactance. We investigated a static random access memory (SRAM) cell and one cross-sectionally prepared Si epilayer structured sample [2]. The derivative of S11 strongly depends on the dc offset bias. The Si epilayer sample reveals the strongest dependence on f_{ac} and also on the biasing history during the SMM measurements.

[1] F. Michael Serry, Agilent Application Note 5989-8818EN, <http://cp.literature.agilent.com/litweb/pdf/5989-8818EN.pdf>, 2008.

[2] C. Baumgart, M. Helm, H. Schmidt, Phys. Rev. B 80, 085305 (2009).

HL 10.7 Mon 15:30 H13

VLS-grown Vertical Silicon Nanowire FETs — •HESHAM GHONEIM, MIKAEL BJOERK, HEINZ SCHMID, KIRSTEN MOSELUND, SIEGFRIED KARG, WALTER RIESS, and HEIKE RIEL — IBM Research GmbH, IBM Research Zurich, Säumerstrasse 4, 8803 Rüschlikon, Switzerland

Owing to their potential compatibility with existing CMOS technology, silicon (Si) nanowires (NWs) are considered to be one of the most promising candidates for future logic and memory elements. A major advantage is the significantly improved gate control using a Gate-All-Around (GAA) structure offered by the NW geometry allowing further downscaling beyond the 22nm node.[1] We report on the fabrication and characterization of vertical Field Effect Transistors (FETs) and vertical impact-ionization FETs based on Vapor-Liquid-Solid (VLS) grown Si NWs. Taking advantage of the vertical epitaxial VLS growth of Si NWs we fabricate GAA devices in a vertical geometry. For source and drain doping we investigated several approaches: in-situ doping during VLS-growth, ion implantation and solid source diffusion doping for both n- and p-type doping. With these methods n-i-n, p-i-p and n-i-p vertical nanowire structures are fabricated and used as basis for p-FETs, n-FETs and impact-ionization FETs. Electrical characteristics of the devices are investigated and a comparison between the different approaches and structures will be discussed.

[1]J.-P. Colinge, Multiple-gate SOI MOSFETs, Solid-State Electronics, 2004, Vol. 48, pp. 897-905.