HL 2: Devices I

Time: Monday 10:15–11:15 Location: H13

HL 2.1 Mon 10:15 H13

Improvement of TFET perfomance by spacer technology — •Marc Dressler, Helmut Lochner, Carolin Axt, Ronny Schindler, Josef Biba, Oliver Hammer, Florian Palitschka, Dorota Kulaga-Egger, Rudolf Nüssl, Tanja Stimpel-Lindner, Torsten Sulima, and Walter Hansch — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

Due to the International Technology Roadmap for Semiconductors (ITRS) the successive downscaling leads to various problems. Some of these problems are caused by limited prospects of photo lithography. Despite resolution enhancement technics like phase shift marks or optical proximity correction the ability to create self-adjusting structures below the resolution limit forces increasing attention. In this work lateral Tunnel-FETs were fabricated. The usage of TFETs are also suitable for short channel devices, because its functionality is based on the well known quantum-mechanical effect of band to band tunneling. To solve the problems of small structures some capable technical tricks are used, e.g. the spacer-technology. Due to these spacer most critical structures (e.g. gate) are self-aligned. A protective function for sensitive gate dielectrics is an additional achievement. To challenge the high demands for the following doping via diffusion a nitride-spacer with specific parameters was developed. The differences between this TFET and common lateral devices without spacer are shown by electrical characterization. The results will be confirmed by characterization abilities like SIMS and REM.

HL 2.2 Mon 10:30 H13

Advanced device performance of TFETs by embedded silicon germanium alloys — •Helmut Lochner, Peter Iskra, Martin Schlosser, Dorota Kulaga-Egger, Torsten Sulima, and Walter Hansch — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

Due to increasing problems by downscaling conventional transistor concepts like the MOSFET, the semiconductor industry is searching for promising new device technologies, such as the Tunnel-FET. Making a virtue out of necessity the TFET takes advantage of the band to band tunneling effect, which is constricting conventional devices. Although the leakage currents can be significant reduced, the ON-current requested by the ITRS (International Technology Roadmap for Semiconductors) cannot be fulfilled. In order to solve this demerit, several solutions are discussed. An efficient way to minimize the deficit is to integrate SiGe alloys in the tunneling region. On the one hand the smaller band gap of SiGe yields in a smaller tunneling gap and consequently in a higher tunnel probability. On the other hand the strained SiGe layer acts as a diffusion barrier. As a consequence the maximum doping concentration at the tunnel region and the sharpness of the doping profile are increasing hand by hand with the resulting ON current. To verify these effects, several TFETs featuring different alloys were fabricated. Electrical measurements like input and output characteristics are confirming these conclusions. The theoretical boarders are pointed out by means of numeric simulations.

HL 2.3 Mon 10:45 H13

SOD as self-acting passivation for lateral TFETs — •Carolin Axt, Helmut Lochner, Marc Dressler, Ronny Schindler, Josef Biba, Rudolf Nüssl, Torsten Sulima, and Walter Hansch — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

According to the ITRS (International Technology Roadmap for Semiconductors)the TFET is a promising successor of the MOSFET. The major problems of current MOSFETs are caused by short channel effects, which results in high OFF-currents. The TFET reverses these unfavorable tunnel currents into useful trait. To investigate new device concepts lateral TFETs were fabricated. Because TFET action is closely connected with extremely high-doped surface layer for source/drain, we used Spin-On-Dopand (SOD) technics. In the common process flow, the SOD-layer has to be removed difficult without affecting the gate oxide. In a changed technological process sequence we used the SOD layer as isolation instead of removing it. The loss of solvent caused by thermodiffusion might result in cracks within the SOD-layer. Metal can enter these cracks while depositing and structuring the contacts. As a result, a short circuit between source or drain and gate are caused. Therefore, photo-resist was implemented to serves as an additional passivation, which ensures a plenary insulation of the doped areas. The results of these transistors with a combined SOD-resist passivation were compared with other lateral TFETs by electrical characterization. Input and output characteristics as well as SIMS measurements and REM graphics are shown.

HL 2.4 Mon 11:00 H13

Properties of an interface layer created by Boron-SOD diffusion — •Ronny Schindler, Josef Biba, Marc Dressler, Carolin Axt, Helmut Lochner, Dorota Kułaga-Egger, Tanja Stimpel-Lindner, Florian Palitschka, Oliver Hammer, Torsten Sulima, and Walter Hansch — Universität der Bundeswehr München, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

The common manner of doping silicon in industry is ion implantation. Besides the high costs this doping method has problems to create shallow surface doping layers as they will be needed for future device generations. We investigate an alternative doping by using Spin-On-Dopants (SOD), where a dopant consisting liquid oxide is deposited on the silicon surface. After solidification the dopant atoms (boron, phosphorous) are driven from the oxide into the silicon by high-temperature diffusion process. As previous experiments have shown, phosphorus performs well, but if boron is used, an etch-resistant layer is left after the process on the surface. The nature and properties of this layer have not been investigated for a full understanding, but it creates problems in device fabrication. For clarification of this problem we fabricated MOS-diodes by using SOD. We tried to find out, if and how this layer can be removed, by using dry etching and wet etching methods. Finally we characterized the different diodes electrically, with and without this layer, to compare which removal technique is the most effective and how strong the influence of this layer is.