T 73: DAQ-Systeme

Zeit: Mittwoch 16:45–19:00 Raum: VG 1.102

T 73.1 Mi 16:45 VG 1.102

ROD DSP Entwicklung innerhalb des IBL Upgrade Projektes — Jörn Grosse-Knetter, •Nina Krieger und Arnulf Quadt — II. Physikalisches Institut, Georg-August-Universität Göttingen

Die jetzige innerste Lage des ATLAS Pixel Detektors ist mit einer Distanz von 5 cm zum Wechselwirkungspunkt der Proton-Proton Strahlen einer hohen Strahlendosis ausgesetzt. Nach einigen Jahren LHC Laufzeit wird daher die Vertexauflösung erheblich nachlassen. Um diesem entgegenzuwirken, wurde eine neue B-Lage IBL geplant, die in den jetzigen Pixel Detektor eingeschoben werden kann. Innerhalb dieses Projektes wurde ein neuer Auslesechip FEI4 und eine neue Auslesekette entwickelt. Letztere besteht unter anderem aus einer Auslesekarte ROD. Der auf dieser Karte befindliche DSP Chip generiert Kommandosignale, die direkt an den neuen Chip gesendet werden. Der Vortrag stellt die ersten Tests mit dem neuen IBL ROD, insbesondere dem DSP, vor. Weiterhin wird auf die Anpassung der DSP Firmware an den neuen Auslesechip FEI4 eingegangen.

T 73.2 Mi 17:00 VG 1.102

Design und Aufbau der Online-PC-Farm des NA62-Experiments am CERN — •Jonas Kunze — Universität Mainz

Das NA62-Experiment stellt als Präzisionsexperiment mit einem kontinuierlichen Strahl ungewöhnliche Anforderungen an das Trigger-System. Während des ca. 5 Sekunden andauernden Strahls fallen über 100 TB an Rohdaten an. Diese müssen anschließend innerhalb der nächsten 15 Sekunden prozessiert sein, bevor erneut neue Daten anfallen. Durch diese zeitversetzte Datenverarbeitung ist, im Vergleich zu Collider-Experimenten mit festen Bunch-Crossing-Raten, beim NA62-Experiment eine effiziente Ausnutzung der Ressourcen nur mit unkonventionellen Methoden möglich. Der Vortrag gibt einen Überblick über die dafür gefundenen Lösungen.

T 73.3 Mi 17:15 VG 1.102

The Data Handling Processor(DHP) for the DEPFET Pixel Vertex Detector — •Mikhail Lemarenko, Tomasz Hemperek, Hans Krüger, and Norbert Wermes — Universität Bonn, Bonn, NRW

A major upgrade of the current Japanese B-Factory (KEKB) is planned by the fall of 2015. Together with this new machine (SuperKEKB), also a new detector, BelleII, will be operated to fully exploit the higher luminosity, 40 times larger than the previous experiment. One of the major changes in the new experiment will be the introduction of a new sub-detector, close to the interaction point, to allow a precise reconstruction of the decay vertices of the B meson systems. This pixel detector, based on the DEPFET technology, will consist of 20 modules arranged in two cylindrical layers around the beam pipe. Each of the modules will be read-out independently by a combination of analog and digital ASICs placed at both ends of each sensor. The digital chip, the Data Handling Processor (DHP), is designed to control the readout chain and to pre-process and compress the data. The chip structure and the latest results will be presented.

In this talk a general overview of the DEPFET sensor with a focus on the DATA processing part, i.e. DHP chip development, will be presented.

T 73.4 Mi 17:30 VG 1.102

FPGA Based Data Reduction Algorithm for the Belle-II DEPFET Detector — •David Münchow, Sören Fleischer, Thomas Gessler, Wolfgang Kühn, Jens-Sören Lange, and Björn Spruck — II. Physikalisches Institut, Universität Gießen

for the Belle-II PXD Collaboration

The readout system of the pixel detector (PXD) at the future Belle-II experiment will have to cope with an estimated input data rate of $\leq$ 21.6 GB/s. The hardware platform of the readout system is going to be ATCA-based Compute Node (CN) with Xilinx Virtex-5 FX70T FPGAs. The large data rate must be reduced by a factor $\sim$ 10 before being send to the event builder. The reduction is done by a region-of-interest (ROI) algorithm based upon e.g. track finding on the high level trigger (HLT).

The free/occupied buffer management, ROI selection, and data unpacking algorithms, programmed in VHDL for the FPGAs, will be explained in detail. Performance results for 100/200 MHz clocks and 32/64 bit bus width will be presented.

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T 73.5 Mi 17:45 VG 1.102

Data Concentrator for the BELLE II DEPFET Pixel Detector — •Michael Schnell, Carlos Mariñas, and Jochen Dingfelder — Physikalisches Institut, Universität Bonn

The innermost two layers of the BELLE II detector located at the KEK facility in Tsukuba, Japan, will be covered by high granularity DEPFET pixel (PXD) sensors. This leads to a high data rate of around 60 Gbps, which has to be significantly reduced by the Data Acquisition System. To perform the data reduction the hit information of the surrounding silicon strip detector (SVD) is used to define so-called Regions of Interest (ROI) and only hits inside these ROIs are saved. The ROIs are computed by reconstructing track segments from SVD data. A data reduction of up to a factor of 10 can be achieved this way. All the necessary processing stages, the receiving and multiplexing of the data on many optical links from the SVD, the track reconstruction and the definition of the ROIs, are performed by the Data Concentrator. The planned hardware design is based on a distributed set of Advanced Mezzanine Cards (AMC) each equipped with a Field Programmable Gate Array (FPGA) chip.

In this talk, the firmware development of the algorithms and the hardware implementation of the Data Concentrator are discussed. In addition, preliminary studies of track reconstruction algorithms, that could be used for FPGA-based tracking, are presented.

T 73.6 Mi 18:00 VG 1.102

Prototype System Tests of the Belle II PXD DAQ System* — Sören Fleischer[1], •Thomas Gessler[1], Wolfgang Kühn[1], Jens Sören Lange[1], Zhen'An Liu[2], David Münchow[1], Björn Spruck[1], Hao Xu[2], and Jingzhou Zhao[2] — [1]II. Physikalisches Institut, Justus-Liebig-Universität Gießen — [2]Institute of High Energy Physics, Chinese Academy of Sciences

For the Belle II PXD Collaboration.

The data acquisition system for the Belle II DEPFET Pixel Vertex Detector (PXD) is designed to cope with a high input data rate of up to 21.6 GB/s. The main hardware component will be AdvancedTCA-based Compute Nodes (CN) equipped with Xilinx Virtex-5 FX70T FPGAs.

The design for the third Compute Node generation was completed recently. The xTCA-compliant system features a carrier board and 4 AMC daughter boards.

First test results of a prototype board will be presented, including tests of (a) The high-speed optical links used for data input, (b) The two 2 GB DDR2-chips on the board and (c) Output of data via ethernet, using UDP and TCP/IP with both hardware and software protocol stacks.

*This work is supported by BMBF under grant 05H10RG8.

T 73.7 Mi 18:15 VG 1.102

Fast serial data transmission for the DEPFET Belle II pixel detector — •Manuel Koch, Carlos Mariñas, Hans Krüger, and Norbert Wermes — Universität Bonn

A two layer vertex pixel detector, built based on the DEPFET technology, is the core component for the Belle II experiment at the super flavor factory SuperKEKB in Japan. The pixel detector produces an estimated total zero-supressed data rate of 256 Gbit/s, which is to be transmitted over 160 high speed links with an individual rate of 1.6 Gbit/s each. Challenges for the design of the serial links include a transmission distance exceeding 15 m, a radiation hard material selection, and high attenuation due to available material budget and space constraints. Modern transmission techniques including pre-emphasis and equalization are necessary to achieve a reliable data transmission; similarly are precise measurements and simulation model extractions needed for the characterization of all high-speed interconnect components. This talk summarizes the challenges, design efforts, and results of the DEPFET collaboration for the high-speed data transmission lines.

T 73.8 Mi 18:30 VG 1.102

Upgrade der Backend-Ausleseelektronik für den LHCb Ou-

ter Tracker — •Stefan Swientek — Experimentelle Physik 5, TU Dortmund

Das kommende Upgrade des LHCb Detektors erfordert eine Erneuerung der Ausleseelektronik. Durch diese soll eine Verarbeitung aller Ereignisse bei einer Bunch-Crossing-Rate von 40 MHz ermöglicht werden.
Gezeigt werden die Pläne für eine derartige Auslese des LHCb Outer Tracker auf dem sogenannten TELL40-Board. TELL40 bezeichnet die Weiterentwicklung der momentan verwendeten Backend-Komponente. Außerdem wird eine an der TU Dortmund entwickelte Erweiterungskarte für Testsysteme mit Stratix IV PCIe Boards vorgestellt. Diese Karte stellt acht optische Transceiver zur Verfügung um realitätsnahe Testbedingungen zu schaffen.

T 73.9 Mi 18:45 VG 1.102

The CTA Medium Size Telescope Prototype, a Test Bench for the Array Control Software. — •Emrah Birsin[1,3], Bagmeet Behera[2], Hendryk Köppel[2], David Melkumyan[2], Igor Oya[1], Torsten Schmidt[2], Ullrich Schwanke[1], Peter Wegner[2], Stephan Wiesand[2], and Michael Winde[2] — [1]Institut für Physik, Humboldt-Universität zu Berlin, Newtonstrasse 15, D-12489 Berlin, Germany — [2]Deutsches Elektronen-Synchrotron, DESY, Platanenallee 6, D-15738 Zeuthen, Germany — [3]for the CTA consortium

CTA (Cherenkov Telescope Array) will be the largest ground-based gamma-ray observatory ever built. Two arrays are foreseen to be build, one in the Southern and one in the Northern hemisphere. A prototype for the Medium Size Telescope (MST) type (diameter: 12 m) will be installed in Berlin in early 2012. This MST prototype will be composed of the mechanical structure, drive system and mirror facets with an active mirror control system. The stability of the mechanical structure will be investigated with CCD cameras and a weather station. Furthermore the ALMA Common Software (ACS) distributed control framework will used as readout and control system for the MST, allowing to evaluate the software with the future use for the whole CTA array in mind. The design of the control software is following the concepts and tools under evaluation within the CTA consortium, like the use of a UML based code generation framework for ACS component modeling, and the use of OPC Unified Architecture (OPC UA) for hardware access. In this contribution the progress in the implementation of the control system for this CTA prototype telescope is described.