HL 65: Devices

Time: Wednesday 11:30–13:15 Location: POT 151

HL 65.1 Wed 11:30 POT 151

Influence of Charge Trapping on Memory Characteristics of Si:HfO2-Based Ferroelectric Field Effect Transistors — •Milan Pešić[1], Stefan Mueller[1], Stefan Slesazeck[1], Alban Zaka[2], Tom Herrmann[2], Ekaterina Yurchuk[1], Uwe Schröder[1], and Thomas Mikolajick[1] — [1]NaMLab gGmbH / * IHM TU Dresden, Dresden, Germany — [2]GLOBALFOUNDRIES Dresden Module One LLC & Co. KG, Dresden, Germany

The Ferroelectric field effect transistors (FeFET) devices have never reached maturity due to limited scalability, low retention and CMOS incompatibility. Only recently, these obstacles seem to have been resolved by the discovery of ferroelectric properties in silicon doped hafnium dioxide (Si:HfO2). This concept proven that possess the potential of realizing highly-scaled ultra low-power memory cells.

One of the main challenges in Si:HfO2 FeFET implementation is the memory window degradation caused by charge trapping effects. In order to analyze the interplay between ferroelectric switching and parasitic charge trapping, a FeFET model including nonlocal tunneling, charge trapping and ferroelectric switching effects was implemented in TCAD Sentaurus Device.

The charge trapping model was qualitatively calibrated based on electrical characterization of Si:HfO2-FeFETs fabricated on a 28 nm bulk technology. From the characterization results, simulation parameters were extracted. In our study we present how bulk traps inside the ferroelectric (Si:HfO2) as well as interface traps at the SiO2 / silicon bulk substrate interfere with the ferroelectric memory characteristics.

HL 65.2 Wed 11:45 POT 151

Non-volatile capacitance change in BiFeO3-coated photocapacitive MIS diodes — •l p Selvaraj[1], t You[1], v John[1], h Zeng[2], d Bürger[1], i Skorupa[1], a Lawerenz[3], o g Schmidt[1,4], and h Schmidt[1] — [1]Faculty of Electrical Engineering and Information Technology, Chemnitz University of Technology, 09107 Chemnitz, Germany — [2]State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, 610054 Chengdu, China — [3]CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH, 99099 Erfurt, Germany — [4]Institute for Integrative Nanosciences, IFW Dresden, 01069 Dresden, Germany

Metal-BiFeO3-metal thin film structures can be switched between a high resistance state (HRS) and a low resistance state (LRS), when a positive and negative writing bias is applied, respectively. The current investigation deals with the effect of light-irradiation on the capacitance of BiFeO3-coated metal-insulator-semiconductor (MIS) diodes. N-type conducting BiFeO3 thin films of nominal thickness 70, 140, 210, 280, 350 and 490 nm have been grown by pulsed laser deposition on p-type silicon wafers substrates having an 163 nm thick SiN layer. The DC bias for the capacitance measurements was swept from +10 V to -15 V and back under different light-irradiation at a sweep rate of ca. 59 mV/s. It has been found that under dark conditions two nonvolatile capacitance minima can be found at -3.8 V and at -6.8 V possibly when the BiFeO3 is in the HRS and LRS state, respectively. The retention measurement result shows non-volatile memory in capacitance which can be used for photocapacitive detectors.

HL 65.3 Wed 12:00 POT 151

RF- and DC Characterization of the High-k to InGaAs Interface in Gate Last nMOSFETs — •Guntrade Roll, Mikael Egard, Sofia Johansson, Erik Lind, and Lars-Erik Wernersson — EIT, Lund University, Lund, Sweden

InGaAs MOSFETs are a promising candidate for low power and high-frequency application. Due to high-injection velocity and mobility it is possible to reach high on-currents at low source/drain voltages. An improved high-k to channel interface quality and low source/drain resistance are challenges currently under research. We have developed a gate last nMOSFET process flow, which gives an excellent extrinsic transconductance of 1.9mS/μm (L_G=55nm) and a source/drain resistance of 199Ω/μm. The presentation will focus on the evaluation of InGaAs/Al_2O_3/HfO_2 interface quality, using RF and DC characteristics. A hopping gate leakage via defects to the transistor raised source/drain is observed. Prestress border defects are filled by trapping when the transistor is turned on. This leads to a transconductance frequency dispersion and current-voltage hysteresis. Reliability is a key issue for all future technologies. The degradation after constant gate stress and hot carrier stress is analyzed. The border trap density is increased by constant gate stress. The threshold bias shift due to trapping is the main reliability problem, which has to be overcome by further improving the high-k processing.

HL 65.4 Wed 12:15 POT 151

Subnanosecond relaxation of free carriers in compensated n- and p-type germanium — •Nils Dessmann[1], Sergey Pavlov[2], Valery Shastin[3], Roman Zhukavin[3], Veniamin Tsyplenkov[3], Stephan Winnerl[4], Martin Mittendorff[5], Nikolai Abrosimov[6], Helge Riemann[6], and Heinz-Wilhelm Hübers[1,2] — [1]Technische Universität Berlin, Berlin, Deutschland — [2]Deutsches Zentrum für Luft- und Raumfahrt, Berlin, Deutschland — [3]Institute for Physics of Microstructures, Nizhny Novgorod, Russland — [4]Helmholtz-Zentrum Dresden-Rossendorf, Dresden-Rossendorf, Deutschland — [5]Technische Universität Dresden, Dresden, Deutschland — [6]Leibniz-Institut für Kristallzüchtung, Berlin, Deutschland

The relaxation of free holes and electrons in highly compensated germanium doped with gallium (p-Ge:Ga:Sb) and antimony (n-Ge:Sb:Ga) has been studied by a pump-probe experiment with the free-electron laser FELBE at the Helmholtz-Zentrum Dresden-Rossendorf. The relaxation times vary between 20 ps and 300 ps and depend on the incident THz intensity and compensation level. The relaxation times are about five times shorter than previously obtained for uncompensated n-Ge:Sb and p-Ge:Ga. The results support the development of fast photoconductive detectors in the THz frequency range.

HL 65.5 Wed 12:30 POT 151

Nickel-related defects and their interaction with H in n- and p-type Si. — •Leopold Scheffler[1], Vladimir Kolkovsky[1], Philipp Saring[2], and Jörg Weber[1] — [1]Technische Universität Dresden, 01069 Dresden, Germany — [2]Georg-August-Universität Göttingen, Friedrich-Hund-Platz 1, 37077 Göttingen, Germany

In the present study we focus our attention on Ni-related defects in n- and p-type Si and investigate their interaction with H. Previously, three dominant deep level transient spectroscopy (DLTS) peaks with the activation energies of EC-0.08 eV (E45), EC-0.4 eV (E230) and EV+0.17 eV (H80) were assigned to the double acceptor, single acceptor and single donor states of substitutional Ni. [1,2] However, in our study the concentration profiles of E45 and E230 were found to be different both in samples with a nickel concentration of NNi ˜ 1x1013cm-3 and NNi ˜ 6x1013cm-3 as determined from E230. This observation suggests a different origin of the dominant DLTS peaks in Ni-doped Si. After wet chemical etching or a dc H plasma treatment a number of additional minor peaks appear in the DLTS spectra. We will show that these peaks are correlated with H and some of them could be assigned to NiH-related complexes. The origin of these defects will be discussed.

[1] M. Shiraishi, J.-U. Sachse, H. Lemke, and J. Weber, Mater. Sci. Eng. B 58, 130 (1999)

[2] H. Kitagawa and H. Nakashima, Jpn. J. Appl. Phys. 28, 305 (1989)

HL 65.6 Wed 12:45 POT 151

Brittle to Ductile transition in silicon nanopillars — •Anton Davydok[1], Thomas W. Cornelius[1], Zhe Ren[1], Francesca Mastropietro[1], Michael Texier[1], Christophe Tromas[2], Ludovic Thilly[2], Marie-Ingrid Richard[1,3], and Olivier Thomas[1] — [1]IM2NP, Marseille, France — [2]PPrime institute, Poitiers, France — [3]ID01 beamline, ESRF, Grenoble, France

In recent years, nanostructures attracted enormous attention due to novel properties which, are not observed for bulk materials. When the object size becomes comparable to intrinsic length scales, finite-size and quantum size effects occur influencing the physical properties. For instance, while bulk silicon is brittle at ambient conditions and ductile at elevated temperatures, Si nanopillars of sufficiently small diameter are ductile at room temperature. In this work, we report on studies of the brittle-to-ductile transition of Si nanopillars as a function of their diameter. Pillars of various sizes were fabricated by electron beam lithography on a Silicon-on-insulator wafer and mechanically deformed employing a nano-indenter. Their structure and defects

induced by the deformation were investigated by electron microscopy as well as by micro- and nanofocused X-ray diffraction. In addition, preliminary finite-element method calculations will be presented.

HL 65.7 Wed 13:00 POT 151

The consecutive photoresponse performance of porous silicon carbide ultraviolet photodetectors — •Nima Naderi[1,2] and Md Roslan Hashim[2] — [1]Division of Semiconductors, Materials and Energy Research Center, Karaj, Iran — [2]Nano-Optoelectronics Research Laboratory, School of Physics, Universiti Sains Malaysia, Penang, Malaysia

This work reports on improvement in the optical and electrical properties of ultraviolet (UV) photodetectors based on porous silicon carbide (PSC). Porous samples were prepared through the optimization of the current density in the UV-assisted electrochemical etching of n-type silicon carbide (SiC) substrates. The current density can be considered an important parameter in controlling the etching rate and morphology of the porous samples. Thus, it can be used to enhance the optical properties of electrochemically etched PSC layers. Therefore, the electrical properties of PSC-based photodetectors such as response time and recovery time can be controlled by optimization of current density in the photoelectrochemical etching of SiC substrate.