HK 60: Instrumentation XVII

Zeit: Donnerstag 16:30–18:30 Raum: S1/01 A4

HK 60.1 Do 16:30 S1/01 A4

Towards new analog read-out electronics for the HADES drift chamber system — •Michael Wiebusch for the HADES-Collaboration — Goethe-Universität, Frankfurt

Track reconstruction in HADES is realized with 24 planar, low-mass drift chambers (MDC). About 27000 drift cells provide precise spatial information of track hit points together with energy loss information, serving for particle ID. In order to handle high rates and track densities required at the future SIS100 accellerator at FAIR, an upgrade of the MDC system is necessary, i.e. by receiving additional redundant layers of drift cells in front of the magnet. This involves new front-end electronics, as the original analog read-out ASIC (ASD8) is no longer in stock and cannot be produced due to its legacy silicon process. Employing new FEE would allow to further increase the sensitivity, e.g. providing additional valuable information for the analysis. This contribution presents a market analysis of alternative state-of-the-art technologies for the analog read-out of drift chambers. Test procedures to evaluate the suitability for the HADES MDCs are discussed and preliminary results are shown. Emphasis is put on the benefits and possible implementations of using two separate analog channels for reading out a sense wire, i.e. a fast amplifier with a discriminator for recording the arrival time of the signal pulse and a slow integrating amplifier with a time-over-threshold discriminator to measure the total charge of the pulse. This work has been supported by BMBF (05P12RFGHJ, 05P15RFFCA), GSI and HIC for FAIR.

HK 60.2 Do 16:45 S1/01 A4

PADI ASIC for straw tube read-out — •Jerzy Pietraszko[1], Michael Träger[1], Jochen Frühauf[1], Christian Schmidt[1], and Mircea Ciobanu[2] for the CBM-Collaboration — [1]GSI, Darmstadt, Germany, — [2]ISS Bucharest, Romania

A prototype of the CBM MUCH straw tube detector[1] consisting of six individual straws of 6mm inner diameter and 220 mm length filled with Ar/CO2 gas mixture has been tested at the COSY accelerator in Jülich. The straw tubes were connected to the FEET-PADI6-HDa PCB[2] equipped with PADI-6 fast amplifier/discriminator ASIC. As a reference counter in this measurement the scCVD diamond detector[3] has been used delivering excellent timing, time resolution below 100ps (sigma), and very precise position information, below 50 μm. The demonstrated position resolution of about 160 μm of the straw tube read out with PADI-6 ASIC confirms the capability of the PADI chip and puts this development as a very attractive readout option for straw tubes and wire chambers.

[1] V. Peshekhonov et al., "Straw tube subsystem of the CBM muon detector", Physics of Particles and Nuclei Letters, March 2012, Volume 9, Issue 2, pp 172-179.

[2] M. Ciobanu et al., "PADI, an ultrafast Preamplifier - Discriminator ASIC for Time of Flight Measurements", Nuclear Science, April 2014, IEEE Transactions ,Volume 61, Issue 2, pp 1015-1023.

[3] J. Pietraszko et al., "Diamonds as timing detectors for minimum-ionizing ...", NIM A 618(2010)121-123

HK 60.3 Do 17:00 S1/01 A4

QDC and TDC for understanding QGP — •Adrian Rost — TU Darmstadt

A flexible COME & KISS Charge-to-Digital-Converter (QDC) and Time-to-Digital-Converter (TDC) read-out scheme will be presented. It will be used for read-out of calorimeters equipped with photo-multiplier tubes (PMTs) or with multi-pixel avalanche photo-diodes (MAPDs) in the HADES and CBM experiments at GSI and the future FAIR facility in Darmstadt.

The detector input signals are integrated with the help of simple analogue electronics (KISS: **K**eep **i**t **S**mall and **S**imple). Afterwards the charge measurement is transformed into a Time-over-Threshold (ToT) measurement using a commercial (COME: Use **Com**mercial **E**lements) FPGA as a discriminator. The well-established TRBv3 platform will provide a very precise ($\sigma_t < 12\,\mathrm{ps}$) FPGA TDC for a ToT measurement of the discriminated signals.

An 8-channel prototype board PaDiWa-AMPS was manufactured and successfully tested in the laboratory and under beam conditions. Beam tests and the optimization process for the HADES ECAL detector will be shown. The adaption of the read-out chain to the NA61/SHINE PSD hadron calorimeter at CERN will also be shown.

This work has been supported by VH-NG-823, Helmholtz Alliance HA216/EMMI and GSI.

HK 60.4 Do 17:15 S1/01 A4

Digital signal processing applied to fast timing measurements with scintillating detectors — •Guillermo Fernández Martínez, Alexander Ignatov, Stoyanka Ilieva, and Thorsten Kröll — Institut für Kernphysik, Technische Universität Darmstadt, Schlossgartenstr. 9, 64289 Darmstadt

In the last few years, new scintillation materials (like $LaBr_3$(Ce) and $CeBr_3$) have been proved to be very appropriate detectors for fast timing measurements, due to their combination of good energy and time resolution with high efficiency. At the same time, the emergence of fast digitisers, that allow for the collection of data at increasingly higher sampling frequencies and are easily scalable to large arrays, such as FATIMA@FAIR, has favoured the transition from traditional, analogue time pick-off methods towards pure digital ones. In our work, we present the results of time resolution measurements with standard radioactive sources, with new, purely digital methods through pulse shape analysis.

HK 60.5 Do 17:30 S1/01 A4

FPGA-Based Upgrade of the Read-Out Electronics for the Low Energy Polarimeter at COSY/Jülich — •Nils Hempelmann for the JEDI-Collaboration — Institut für Kernphysik, Forschungszentrum Jülich

The Cooler Synchrotron (COSY) is a facility for cooled polarized beams at the Forschungszentrum in Jülich. The Low Energy Polarimeter (LEP [1,2]) is the polarimeter in the injection beam line of COSY [3]. The beam polarization is measured using scattering off carbon and polyethylene (CH2) targets. The outgoing particles are detected using twelve plastic scintillators installed in groups of three to the left, to the right, above, and below the beam. The LEP is the routine tool for beam set-up, but its performance was limited by the old read-out electronics consisting of analog NIM modules. A new system using analog pulse sampling and an FPGA chip for signal processing was installed and tested. The ejectile particles were identified by relative time of flight measurement using a signal from the RF amplifier of the cyclotron used for acceleration as a reference. The new system is able to measure the time at which a particle arrives to an accuracy in the order of 50 ps. The presentation includes a review of available systems and a report about measurements in May and December 2015.

[1] M. Eggert, Entwicklung eines gepulsten Casium-Ionenstrahls fur die Quelle polarisierter Ionen an COSY/Julich, PhD Thesis, 1998 [2] N. Hempelmann, FPGA-Based Upgrade of the Read-Out Electronics for the Low Energy Polarimeter at COSY/Jülich, Presentation at PSTP Bochum, 2015 [3] R. Maier, Nucl. Instr. and Meth. A 390 (1997) 1

HK 60.6 Do 17:45 S1/01 A4

The read-out chain of the CBM STS detector — •Jörg Lehnert and David Emschermann for the CBM-Collaboration — GSI Helmholtzzentrum für Schwerionenforschung GmbH

The Compressed Baryonic Matter (CBM) experiment at FAIR will explore the QCD phase diagram at high baryon densities during nucleus-nucleus collisions in a fixed target setup. Its physics goals require interaction rates up to 10 MHz, which can be exploited with fast and radiation hard detectors equipped with free-streaming front-end and readout electronics, connected to a common Data Aquisition (DAQ) system to forward data to the First Level Event Selector (FLES). The core component of the CBM DAQ system is the Data Processing Board (DPB) implementing three important functionalities:

- The incoming data via multiple lower-speed, short distance links is preprocessed, concentrated and forwarded to the FLES via higher-speed, long distance links.
- The DPBs provide an interface for the Detector Control System (DCS) to configure readout and front-end electronics (FEE).
- As part of the Timing and Fast Control (TFC) system the DPBs ensure transmission of the reference clock and synchronous commands necessary to synchronize the FEE.

This contribution will present the readout and DAQ chain on the example of the core subdetector, the Silicon Tracking System (STS).

HK 60.7 Do 18:00 S1/01 A4

Thin and Reliable Connectivity for the CBM-MVD — •Philipp Klaus for the CBM-MVD-Collaboration — Institut für Kernphysik, Goethe-Universität Frankfurt

The CBM Micro Vertex Detector requires reliable connectivity to its ∼ 300 CMOS Monolithic Pixel Sensors (CPS). This includes stable powering but also reliable data transmission and fault tolerance. Another requirement is to keep the material budget to a minimum as the cables will be partially in the acceptance of the micro vertex detector. This contribution will summarize our current efforts to reduce the material budget of the readout cables while ensuring reliable connectivity. Our latest prototype of the second station of the MVD (named PRESTO) was studied to obtain the presented results.
*This work has been supported by BMBF (05P12RFFC7), H-QM, HIC for FAIR und GSI.

HK 60.8 Do 18:15 S1/01 A4

Implementation of the ALICE HLT hardware cluster finder algorithm in Vivado HLS — •Frederik Grüll, Heiko Engel, and Udo Kebschull for the ALICE-Collaboration — Infrastructure and Computer Systems in Data Processing, Goethe University Frankfurt, Germany

The FastClusterFinder algorithm running in the ALICE High-Level Trigger (HLT) read-out boards extracts clusters from raw data from the Time Projection Chamber (TPC) detector and forwards them to the HLT data processing framework for tracking, event reconstruction and compression. It serves as an early stage of feature extraction in the FPGA of the board. Past and current implementations are written in VHDL on reconfigurable hardware for high throughput and low latency. We examine Vivado HLS, a high-level language that promises an increased developer productivity, as an alternative. The implementation of the application is compared to descriptions in VHDL and MaxJ in terms of productivity, resource usage and maximum clock frequency.