HK 63: Instrumentation XIV

Zeit: Freitag 14:00–16:00 Raum: F 072

HK 63.1 Fr 14:00 F 072

A phoswich detector readout with GHz sampling using the FEBEX platform — Roman Gernhäuser, Benjamin Heiss, Philipp Klenze, Patrick Remmels, •Felix Stark, and Max Winkel — Technische Universität München

The most forward part of the CALIFA Calorimeter consists of very fast LaBr3/LaCl3 scintillation crystals in a Phoswich configuration. To separate both components of the scintillation light with a spectroscopic resolution, the signals have to be sampled with rates of about 1 GSPS and 14 bits resolution at least. A new frontend electronics based on the DRS4 chip will provide buffered analogue signals. A direct connection to the CALIFA data acquisition platform FEBEX will allow for a homogeneous integration into the existing R3B-DAQ. Using two different ADC channels for each detector unit provides a straight forward use of the DRS4 in a free running self triggered system. We will present the readout concept, its implementation and a series of detailed tests of a first prototype which has been recently developed. Supported by BMBF Project 05P15WOFNA.

HK 63.2 Fr 14:15 F 072

Test of the STS-XYTER2 frontend ASIC for the CBM Silicon Tracking System — •Adrian Rodriguez Rodriguez[1,2] and Jörg Lehnert[2] for the CBM-Collaboration — [1]Goethe Universität Frankfurt am Main — [2]GSI Helmholtzzentrum für Schwerionenforschung

The Silicon Tracking System (STS) is the essential tracking component of the CBM experiment. The STS-XYTER2 is the prototype ASIC dedicated for reading out the double-sided sensors of the STS. It is a low power, self-triggering ASIC which generates timing and energy information for each sensor signal. After tests of the previous prototype, the chip design was revised. The current ASIC version implements various improvements to achieve the desired noise levels, and ensure fail-safe operation. The digital backend was completely re-designed. A new readout protocol was developed and implemented for operation with the GBTx data concentrator. Several tests are carried out to check chip functionalities, performance, and system integration aspects. An overview of the experimental setup, device tests and results will be presented.
Supported by HGS-HIRe.

HK 63.3 Fr 14:30 F 072

Reliable experimental physics DCS Board program execution with COTS TMS570 MCU — •Antonio Lucio, Jano Gebelein, and Udo Kebschull — Infrastructure and Computer Systems in Data Processing, Goethe University Frankfurt, Germany

Given the necessity of a Detector Control Systems Board (DCSB), which shall provide 100 GPIOs, SPI, I2C CAN bus and other interfaces for detector parameter surveillance in experimental physics applications, a new DCSB design is being conceived. Furthermore, under the premise of using low Cost Commercial Off The Shelf (COTS) MCU's, reliable program execution from external redundancy-less memory is necessary. For that purpose the safety MCU TMS570 for automotive applications is examined. EPICS, a Commonly used SCADA for physics experiments, is ported to the MCU and specific MCU's mechanisms are used to apply redundancy to programs executing from external memories with insignificant amount of CPU overhead. Data redundancy reliability from such mechanisms is examined and results are displayed.

HK 63.4 Fr 14:45 F 072

First measurements on the new FPGA-based DIRICH MAPMT readout* — •Vivek Patel, Karl-Heinz Kampert, and Christian Pauly — Wuppertal university

The DIRICH module is the core part of a new readout chain for multianode PMTs and MCPs, being developed in a joined effort by the CBM-, HADES- and PANDA collaborations for their respective RICH detectors. The design focuses on excellent timing precision, limited by the Transit Time Spread(TTS) of the sensors (MAPMTs: $\sim$ 300 ps, MCPs: <100 ps). Discriminination, time- and time-over-threshold measurement, as well as digital data handling, are all implemented on a single Lattice ECP5 FPGA, providing a cost-effective and highly compact solution. First prototypes of the DIRICH module are available for testing in the lab, and also using a dedicated test chamber with single photon light source, which will later allow for a complete system test of the new HADES photon detector prior its installation in the HADES RICH. In the talk we will present first tests and performance measurements on the DiRICH.

*Supported by : BMBF grant 05P15PXFCA, and GSI.

HK 63.5 Fr 15:00 F 072

DiRich - Readout Electronics for DIRC and RICH detectors at FAIR — •Jan Michel[1], Vivek Patel[2], Christian Pauly[2], Peter Skott[3], and Michael Traxler[3] for the HADES-Collaboration — [1]Goethe-Universität Frankfurt — [2]Bergische Universität Wuppertal — [3]GSI Helmholtzzentrum Darmstadt

Several experiments at FAIR will make use of Cherenkov detectors, namely the DIRC of the PANDA experiment and the RICH of HADES and CBM. All will be equipped with 64 channel PMTs. The DiRich module is a compact set of read-out electronics that includes all features required for these detectors: The front-end board houses discrete, low-power amplifiers and FPGA-based TDC. Auxiliary boards include a power supply and a data concentrator that provides the connection to the data acquisition system of the detectors using an optical link for data transport. All boards are connected via a 10 by 15 cm sized backplane that doubles as mechanical support for the PMTs and light-tight shielding. We present the electronics along with selected performance test results.

This work has been supported by BMBF grants 05P15PXFCA and 05P15RGFCA and contributions from the TRB3 collaboration.

HK 63.6 Fr 15:15 F 072

Evaluation of the CBM FLES input interface at 2016 CERN/SPS beam test — •Dirk Hutter, Jan de Cuveland, and Volker Lindenstruth for the CBM-Collaboration — Frankfurt Institute for Advanced Studies, Goethe University, Frankfurt, Germany

The CBM First-level Event Selector (FLES) is the central event selection system of the upcoming CBM experiment at FAIR. Designed as a high-performance computing cluster, its task is an online analysis of the physics data at a total data rate exceeding 1 TByte/s. All physics data input to the cluster is handled by a custom input interface. It comprises a custom PCIe FPGA board receiving data via optical links and handling DMA transfers to the PC's memory, an accompanying HDL module implementing the front-end logic interface and link protocol in the front-ends and a software stack publishing data to the subsequent FLES data transport framework in a very efficient way.

Read-out chains for several CBM subsystems have been successfully implemented using prototype components of the input interface. A larger scale evaluation of the FLES input interface and data handling framework has been performed during the 2016 CBM beam test at CERN/SPS. Up to 14 input links from two different subsystems have been synchronously read and archived. The structure of the input interface and FLES datapath matched the foreseen final CBM setup. An overview of the read-out setup and beam test results on system performance will be presented.

HK 63.7 Fr 15:30 F 072

Towards new analog read-out electronics for the HADES drift chamber system — •Michael Wiebusch for the HADES-Collaboration — Goethe-Universität, Frankfurt

Track reconstruction in HADES is realized with 24 planar, low-mass drift chambers (MDC). About 27000 drift cells provide both, precise spatial information of track hit points and energy loss information. In order to handle high rates and track densities required at the future SIS100 accellerator at FAIR, an upgrade of the MDC system is necessary. This involves new front-end electronics, as the original analog read-out ASIC (ASD8) is no longer procurable. A promising replacement read-out chip candidate is the PASTTREC ASIC (developed at Jagiellonian University, Krakow), which is currently at the focus of our investigations. This contribution will present the test procedures employed to evaluate the compatibility of the ASIC with the drift chambers w.r.t. spatial/energy resolution and detection efficiency. Also a cost-efficient and lightweight FPGA-based prototype TDC is used, which is foreseen to replace the TDC ASICs presently used. To arrive at conclusive performance results, the tests have to be conducted un-

der realistic conditions in direct comparison to the present ASICs.
This work has been supported by BMBF (05P15RFFCA), GSI, HGS-HIRe and HIC for FAIR.

HK 63.8 Fr 15:45 F 072

A read-out system for the PANDA MVD prototypes: development and results. — •Alessandra Lai, Tobias Stockmanns, and James Ritman for the PANDA-Collaboration — Forschungszentrum Jülich, Germany

The PANDA experiment will play a key role at the upcoming Facility for Antiproton and Ion Research (FAIR) in Darmstadt. Exploiting proton-antiproton interactions, its scientific program addresses fundamental questions of QCD. The Micro Vertex Detector (MVD) is the sub-detector system closest to the interaction point. It uses two different kinds of silicon detectors as sensitive elements: hybrid pixel detectors and double-sided strip detectors. Two different types of front-end ASICs are under development for the MVD: the Torino Pixel ASIC (ToPix) and the PANDA Strip ASIC (PASTA). Both are designed to transmit untriggered data at a rate of hundreds of Mb/s and handle the expected hit rate in hot spots of the detector. A test system capable of handling these high rates is therefore needed. It should have the flexibility to test different kinds of front-end electronics and be easy to adapt to new prototypes. Therefore, an FPGA-based system is the ideal candidate. Suitable firmware and a software framework are thus under development at the Forschungszentrum Jülich.

In this talk, the mentioned read-out system will be introduced and performance tests with the front-end electronics prototypes of the MVD will be presented.