DS 12: Invited Geer

Time: Tuesday 9:30–10:15 Location: GER 38

Invited Talk DS 12.1 Tue 9:30 GER 38

Nanoscale Profiling of Electron Transport in Metallic and Semimetal films — Chaehwi Chong, Yunfei Wang, and •Robert Geer — College of Nanoscale Science and Engineering, University at Albany, Albany, NY, USA

As lithographic feature sizes in nanoelectronics drop below the electron scattering length for conventional metals, it is essential to characterize nanoscale variations in electron transport due to compositional heterogeneity or interfacial nonuniformity. For conventional nanoelectronics a case in point is ultra-thin barrier layers and interconnect lines in Cu-damascene on-chip wiring. Local two-point conductance profiling via scanning-probe microscopy has been used to quantitatively map electrical side-wall continuity in as-deposited ALD Ta-based barriers (thickness < 2nm) and local electrical transport in Cu interconnects (< 90 nm) on a 300mm wafer back-end-of-line test structure. Nanoscale electrical continuity profiling on Ta barrier films reveal a strong dependence on sidewall topography stemming from lithographic line-edge roughness from cross-correlation analysis. Also, Cu interconnect conductance profiling reveals strong nanoscale variations attributed to local oxidation. These data are compared to FEA modeling for thin-film electron transport. A second case of interest is the use of similar techniques to investigate electron transport in linearly-dispersive semimetals (graphene). Results on exfoliated and CVD graphene deposited on split-gate structures are presented in terms of electrostatic doping for electron current focusing (e.g. Veselago lens) from monolayer graphene. Preliminary results are consistent with model predictions.