HL 21: Devices

Time: Tuesday 14:00–16:00 Location: BEY 81

HL 21.1 Tue 14:00 BEY 81

High-Performance Tunnel Field Effect Transistor (TFET) using ultra-high-k gate dielectrics — •Martin Schlosser, Helmut Lochner, Martin Sauter, Thomas Zilbauer, Torsten Sulima, and Ignaz Eisele — Institute of Physics, Nano and Micro Systems, University of the German Federal Armed Forces Munich, 85577 Neubiberg, Germany

Continuous downscaling of field effect transistors is about to reach physical limits and calls for new device concepts. The Tunnel FET (TFET), based on a gated pin-diode, is a promising candidate for future CMOS technology due to its superior properties like small subthreshold slope, fabrication without sophisticated technology and good temperature stability. However, increasing the on-current remains challenging. We propose to use thick ultra-high-k materials as gate dielectrics in order to induce a higher electric field at the tunnelling junction due to the well-known fringing field effect. While worsening the device characteristics of a conventional MOSFET, it turns out that this effect significantly enhances the device performance of TFET devices. The reason is that the off-current is given by a pin-diode leakage current, while the on-current increases exponentially with the electric field. On-currents fulfilling the actual ITRS roadmap and slopes down to 20 mV/dec are observed in simulations of the device by using a generic dielectric with k = 200 and d = 102 nm. As aggressive downscaling of EOT is not needed, the usability for high-frequency applications is very good due to the low gate capacitance.

HL 21.2 Tue 14:15 BEY 81

Separation and Analysis of different leakage mechanisms in modern MOSFETs — •Guntrade Roll[1], Matthias Goldbach[2], Andre Wachowiak[2], Juergen Holz[2], and Lothar Frey[3] — [1]Namlab Gmbh, D-01187 Dresden — [2]Qimonda, D-01099 Dresden — [3]Fraunhofer IISB, D-91058 Erlangen

CMOS device development via gate length reduction is driven by the requirement for performance enhancement under power consumption control. Gate length scaling is enabled by reducing gate oxide thickness, parasitic capacitances as well as source/drain junction depth. These actions typically lead to increasing device leakage currents.
I will present detailed investigations of leakage currents and mechanisms on industry fabricated PFET devices with channel length smaller 100nm. The influence of the gate induced drain leakage (GIDL), drain induced barrier lowering (DIBL), p+/n-junction- and gate leakage on the total device current loss is studied with temperature dependent current-voltage- and capacitance-voltage-measurements. Two types of sample systems have been investigated:
- PFETs with ultra shallow source/drain (carbon co-implantation)
- PFETs with high-k gate dielectric and metal gate
The analysis reveals the relative magnitude of the different leakage current contributions, the DIBL effect and GIDL control the leakage for increasing drain bias. The underlying mechanisms (direct tunneling, defect assisted etc.) are investigated.

HL 21.3 Tue 14:30 BEY 81

Vertical IMOS with n-doped deltas for high temperature applications — •Tina Kubot, Ulrich Abelein, Peter Iskra, Torsten Sulima, and Ignaz Eisele — Universität der Bundeswehr, Institut für Physik, Werner-Heisenberg-Weg 39, 85577 Neubiberg

The demands for process control in high temperature (HT) environments like engines or exhaust systems grow e.g. due to stricter requirements in CO_2-emission. The low temperature tolerance of common silicon based devices becomes a great issue in the development of suitable sensors and readout electronics. Increased intrinsic charge carrier density and decreased pn-junction barrier height can reduce the device performance down to total failure of the devices.

With the IMOS we have introduced a device concept which has proven its suitability for HT-environments. After realizing p-delta planar doped barrier (PDB) FET structures with superior Drain-Source leakage currents and high On-Off-Ratios at 500 K we now present n-doped PDB-structures. We show investigations on the temperature dependent barrier properties of highly phosphorus doped deltas in p^+-i-$n^+\delta$-i-p^+-diode structures fabricated by molecular beam epitaxy. The deltas have a thickness of 3 nm and a doping level of $> 10^{19}$ cm^{-3}. Temperature dependent I-V-measurements were carried out from room temperature up to 500 K. For the measurements a semiconductor parameter analyzer with a heated chuck was used. The electrical characteristics of these test devices show a good barrier formation by the delta layer even at elevated temperatures.

HL 21.4 Tue 14:45 BEY 81

Characterization of of ZnO and MgZnO MSM Photodectecors — •Lucie Behnke, Zhang Zhipeng, Gisela Biene, Mathias Schmidt, Alexander Müller, Holger v. Wenckstern, Marius Grundmann, and Holger Hochmuth — Fakultät für Physik und Geowissenschaften, Universität Leipzig, Linnéstr. 5, Germany

There is a wide range of applications for small, fast and transparent photodetectors. For their fabrication ZnO is a promising material, because of its large, direct bandgap. We investigated interdigital metal-semiconconductor-metal structures of different Schottky contact metals on $Mg_xZn_{1-x}O$; the concentration of magnesium x varies from 0 to 0,21. The contacts were realized by reactiv DC sputtering, which results in high-quality Schottky contacts. The reproducibility was confirmed by current-voltage measurements of about 80 devices. The detectors were characterized by photocurrent, noise and light beam induced current measurements. Further, we found a correlation between the magnesium concentration and the leakage current. We discuss the quantum efficiency in dependence of x.

15 min. break

HL 21.5 Tue 15:15 BEY 81

Low operation voltage light emitting device based on ZnO nanoparticles — •Ekaterina Neshataeva[1], Tilmar Kümmell[1], André Ebbers[2], and Gerd Bacher[1] — [1]Werkstoffe der Elektrotechnik and CeNIDE, Universität Duisburg-Essen, 47057 Duisburg — [2]Evonik Degussa GmbH, Creavis, 45764 Marl, Germany

Semiconductor nanoparticles are very attractive candidates for future large-area light emitting devices that are both cost-effective and robust. In this contribution we demonstrate a ZnO nanoparticle light emitting device, which operates at low voltages without the need of any organic support layers. Tight nanoparticle layers were fabricated by a spin coating process using commercially available ZnO nanoparticles from the gas phase and fluorine-doped tin oxide glass as a substrate. After evaporation of a top electrode, a diode-like I-V characteristic was obtained. The device operation at room temperature starts at 4V and shows electroluminescence in the visible spectral range and a pronounced UV peak related to near-band gap emission of the ZnO. Thus, our findings open a path towards all-inorganic large-area particle based luminescent devices.

HL 21.6 Tue 15:30 BEY 81

E-Beam alignment markers for high overlay accuracy — •Jürgen Moers[1,2], Julian Gerharz[1,2], Stefan Trellenkamp[1,2], and Detlev Grützmacher[1,2] — [1]Institute for Bio- and Nanosystems, Research Center Jülich, D-52425 Jülich, Gemany — [2]JARA Jülich Aachen Research Alliance

In recent years the dimensions of semiconductor devices have been decreased to the deep sub-100nm range with an overlay requirement of 10nm and below. In research e-beam lithography is used to meet those requirements. The key issue for achieving the overly accuracy is the quality of the alignment markers. For this purpose square holes etched into the silicon substrate are used.

The e-beam tool triggers on the contrast transition between the marker and the surrounding area. The position of this transition is the marker edge. Its position is determined by averaging over several measurements of the contrast transition. The marker position is given by the center of the positions of the four marker edges.

While with new markers an intrinsic overlay of 10nm can be achieved, the quality of the markers deteriorate during processing. In this work the effect of layer deposition, epitaxial growth and etching steps on the overlay accuracy is investigated. It can be shown, that the standard deviation of the determined position of the marker edge increases, while the determined center of the marker is till found in good agreement with its designed position. Hence an overlay of 10 nm can still be achieved.

HL 21.7 Tue 15:45 BEY 81

First prototype of a novel memory device based on self-organized quantum dots — •Andreas Marent[1], Tobias Nowozin[1], Martin Geller[2], Johannes Gelze[1], and Dieter Bimberg[1] — [1]Institut für Festkörperphysik, TU Berlin, Hardenbergstr. 36, 10623 Berlin — [2]Fachbereich Physik und CeNIDE, Universität Duisburg-Essen , Lotharstrasse 1, 47048 Duisburg

We have developed a memory concept (QD-Flash) based on self-organized quantum dots (QDs) [1] with the potential to overcome the restrictions of nowadays most important semiconductor memory, the Flash-memory. The main disadvantage of the Flash-memory results from the use of Si/SiO_2 which leads to a fundamental trade-off between write time and storage time. In contrast, using III-V semiconductors in the QD-Flash, ultra fast write times ($<$ ns) in combination with a long storage time ($>>$ 10 years) can be realized.

We demonstrate a first prototype of the QD-Flash with full functionality using InAs-QDs in $Al_{0.9}Ga_{0.1}As$ as memory units. The performance of the prototype has been evaluated up to room temperature. Read out of the stored information was successfully realized by measuring the resistance of a two-dimenional hole gas formed in a $GaAs/Al_{0.9}Ga_{0.1}As$ quantum well embedded below the QD-layer.

[1] M. Geller, A. Marent, and D. Bimberg, Auf Halbleiter-Nanostrukturen basierender nicht-flüchtiger Speicher "A non-volatile memory based on semiconductor nanostructure", CPT patent application, submitted (2006).