# HK 20: Instrumentierung IV

Time: Tuesday 14:00–16:00 Location: HS1

**Group Report** HK 20.1 Tue 14:00 HS1

**Der BGO-OD-Aufbau an ELSA** — •Oliver Jahn für die BGO-OD-Kollaboration — Physikalisches Institut, University of Bonn, Germany

The new BGO-OD experiment is currently being set up at the electron accelerator facility ELSA of the University of Bonn. It consists of the BGO rugby ball detector of the former GRAAL experiment that covers almost the full solid angle and is supplemented with an open dipole spectrometer magnet and several components with high granularity for high resolution detection of forward going particles, both charged and neutral. These properties allow for the investigation of various final states, especially pseudoscalar, vector meson and associated strangeness photoproduction. This contribution will survey the current status of the setup and its components. (supported by the DFG (SFB/TR-16))

HK 20.2 Tue 14:30 HS1

**Datenerfassung für das BGO-OD Experiment an ELSA *** — •Daniel Hammann für die BGO-OD-Kollaboration — Physikalisches Institut, Universität Bonn

Im Sommer 2011 wird das BGO-OD Experiment an ELSA seinen Betrieb aufnehmen. Zur Untersuchung der Photoproduktion von Mesonen sollen dabei insbesondere gemischt geladene/neutrale Endzustände beobachtet werden. Hierzu besteht der Aufbau aus einem BGO-Kalorimeter, welches den größten Teil des Raumwinkels abdeckt und einem Dipol-Spektrometer in Vorwärtsrichtung. Zur Spurmessung kommen großflächige Driftkammern und szintillierende Fasern zum Einsatz. Eine Szintillatorwand hinter dem Spektrometer dient zur Bestimmung der Flugzeit und damit zur Identifikation der Teilchen. Um die über 4000 Kanäle der unterschiedlichen Detektoren mit einer Ereignisrate von mehreren kHz auslesen zu können, wurde eine leistungsfähige Datenerfassung erstellt, die hier vorgestellt wird.

* gefördert durch die DFG im Rahmen des SFB / TR 16

HK 20.3 Tue 14:45 HS1

**Das Upgrade des HADES Spektrometers*** — •Jan Michel für die HADES-Kollaboration — Institut für Kernphysik, Goethe-Universität Frankfurt am Main

Das High Acceptance DiElectron Spectrometer (HADES) befindet sich am SIS-18 Beschleuniger am GSI Helmholtzzentrum für Schwerionenforschung in Darmstadt und hat während der letzten Jahre verschiedene Experimente mit leichten und schweren Ionen bei Energien von 1 bis 3,5 AGeV/$c^2$ durchgeführt. Nun wurde das Spektrometer mit einer Resistive Plate Chamber (RPC) zur Verbesserung der Granularität und Zeitauflösung sowie einem Vorwärts-Hodoskop erweitert.

In diesem Zusammenhang wurde insbesondere das Datenaufnahmesystem komplett ersetzt, um Ereignisraten von bis zu 20 kHz für Schwerionenkollissionen sowie 100 kHz für leichte Stoßsysteme möglich zu machen. Die neue Elektronik besteht aus FPGA-basierenden Boards, um höchste Datenraten bei niedrigen Latenzen sowie eine hohe Flexibilität in der Frontend-Elektronik zu gewährleisten. Der Datentransport wird hauptsächlich über optische Fasern abgewickelt. Die Konfigurations- und Überwachungsfunktionen wurden durch den Einsatz eines einheitlichen Netzwerkprotokolls erheblich verbessert.

Insgesamt können mit dem neuen System Datenraten von bis zu 250 MByte/s erreicht werden. In diesem Vortrag wird das HADES Upgrade beschrieben, das Datenauslesesystem vorgestellt und Performance-Messungen gezeigt.

*Unterstützt durch BMBF (06FY9100I), EU FP6, GSI, HIC for FAIR und HGS-HIRe.

HK 20.4 Tue 15:00 HS1

**An IPMI-Based Slow Control System for the $\overline{\text{P}}$ANDA Compute Node*** — Martin Galuska, •Thomas Gessler, Wolfgang Kühn, Johannes Lang, Jens Sören Lange, Yutie Liang, Ming Liu, Björn Spruck, and Qiang Wang for the PANDA-Collaboration — II. Physikalisches Institut, Justus-Liebig-Universität Gießen

Reaction rate of 10–20 MHz from antiproton-proton-collisions are expected for the $\overline{\text{P}}$ANDA experiment at FAIR, leading to a raw data output rate of up to 200 GB/s. A sophisticated data acquisition system is needed in order to select physically relevant events online. A network of FPGA-based Compute Nodes will be used for this purpose.

An AdvancedTCA shelf provides the infrastructure for up to 14 Compute Nodes. A Shelf Manager supervises the system health and regulates power distribution and temperature. It relies on a local controller on each Compute Node to relay sensor readings, provide power requirements etc. This makes remote management of the entire system possible. An IPM Controller based on an Atmel microcontroller was designed for this purpose, and a prototype was produced.

The necessary firmware is being developed to allow interaction with the components of the Compute Node and the Shelf Manager conform to the AdvancedTCA specification. A set of basic mandatory functions was implemented that can be extended easily. An improved version of the controller is in development. An overview of the intended functions of the controller and a status report will be given.

* This work was supported in part by the BMBF (06GI9107I) and by HIC for FAIR.

HK 20.5 Tue 15:15 HS1

**A Common Read-Out Receiver Card for ALICE DAQ and HLT** — •Heiko Engel and Udo Kebschull for the ALICE-Collaboration — Kirchhoff-Institut für Physik, Universität Heidelberg

In the ALICE read-out chain, both Data Acquisition (DAQ) and High Level Trigger (HLT) use FPGA-based Read-Out Receiver Cards (RORC) as interface between the optical Detector Data Link (DDL) and the DAQ and HLT cluster machines. The DAQ-RORC and the HLT-RORC have been developed as independent projects with quite similar requirements and are now facing the same problem: Both cards use a PCI-X interface to the host machines, which is not available anymore in current and future PCs. Therefore, a new common RORC for DAQ and HLT is developed. This new RORC will have a fast PCIe interface, high density parallel optical DDL connections and will combine several of the old cards into one new device. The new RORC will be backward compatible to the current protocols and transmission rates and can be integrated seamlessly into the current setup while providing room for DDL speed upgrades and further FPGA-based data pre-processing.

HK 20.6 Tue 15:30 HS1

**The Universal Read-Out Controler for CBM at FAIR** — •Sebastian Manz, Norbert Abel, and Jano Gebelein for the CBM-Collaboration — Kirchhoff-Institut für Physik, Heidelberg, Germany

Since 2007 we design and develop the firmware for the read-out controller (ROC) for data acquisition of the CBM detector at FAIR. While our first implementation solely focused on the nXYTER chip, today we are also designing and implementing readout logic for the GET4 chip which is supposed to be part of the time of flight (TOF) detector.

Furthermore, we fully support both Ethernet and Optical transport as two transparent solutions. This addresses the different requirements of a laboratory setup and the final detector setup respectively.

The usage of a strict modularization of the Read Out Controller firmware enables us to provide an Universal ROC where front-end specific logic and transport logic can be combined in a very flexible way.

Fault tolerance techniques are only required for some of those modules and hence are only implemented there.

HK 20.7 Tue 15:45 HS1

**Experiences and results using the CBMnet protocol including precise time synchronization and clock distribution** — •Frank Lemke, Sven Schenk, and Ulrich Bruening for the CBM-Collaboration — ZITI University of Heidelberg, Mannheim, Germany

Within the context of the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research in Darmstadt a Data Acquisition (DAQ) system has been built using the CBMnet protocol on unified optical connections. For beam time tests in 12/2010 a hierarchical DAQ was built that consisted of 8 Read-Out Controllers (ROC) collecting data from different detectors, attached in groups of 4 to 2 Data Combiner Boards (DCB). Each DCB used an Active Buffer Board (ABB) as data sink and for both another ABB serves as clock distribution and synchronization source. In order to use Deterministic Latency Messages (DLM) for synchronizing the network path to the detectors all clocks within the network had to be derived from one base clock. The arrival of a DLM in a ROC triggers a reset of epoch counters

required by the compute nodes to combine collected data of different ROCs. Clock distribution worked reliably and by reducing the jitter of some recovered clocks to less than 10ps RMS, the goal of deterministic timing and synchronization over optical links has been achieved. The CBMnet protocol, that merges synchronization and clock distribution as well as control messages and detector data into virtual channels on the unified optical link, worked well. The experiences gained and also some new detector requirements lead to new ideas for further refinements such as unbalanced lane handling and long message support.