HK 34: Instrumentation

Zeit: Mittwoch 16:30–19:00 Raum: P 2

Gruppenbericht HK 34.1 Mi 16:30 P 2

Trigger-less readout of the PANDA Electromagnetic Calorimeter — Myroslav Kavatsyuk, Johan G. Messchendorp, Hossein Moeini, •Ganesh Tambave, and Herbert Loehner for the PANDA-Collaboration — KVI, University of Groningen, Zernikelaan 25, NL-9747AA Groningen

Charm-meson resonances and yet undiscovered glueballs might reveal the origin of the hadronic mass spectrum. To this end the PANDA collaboration at FAIR will exploit antiproton annihilations for precision studies of e.g. charmonium resonance states. In order to achieve a highly flexible event selection, a trigger-less data-acquisition system is currently being developed. We have constructed the prototype of a readout chain for the PANDA Electromagnetic Calorimeter (EMC), in order to demonstrate the feasibility of a fast online event selection on basis of high-level physics information. The readout is based on intelligent front-end electronics which autonomously recognises valid hits and extracts the relevant information. The EMC employs a sampling-ADC readout incorporating a pulse-processing algorithm [1], which is able to process data at hit rates up to 500 kHz, and includes the recovery of pile-up pulses. The developed algorithm was applied in the EMC prototype detector[2]. We will describe the functionality of the developed readout chain, present results of test experiments revealing the accuracy of time synchronisation, discuss the performance of the pile-up recovery algorithm, and report on the validation studies of the simulation package. [1] E. Guliyev, et al., NIM A 664 (2012) 22; [2] M. Kavatsyuk et al., NIM A 648 (2011) 77.

Gruppenbericht HK 34.2 Mi 17:00 P 2

Progress on the Compute Node based DAQ System for PANDA — •Björn Spruck[1], Sören Fleischer[1], Thomas Gessler[1], Wolfgang Kühn[1], Jens Sören Lange[1], Zhen'An Liu[2], David Münchow[1], Hao Xu[1,2], and Jingzhou Zhao[2] for the PANDA-Collaboration — [1]II. Physikalisches Institut, Universität Gießen — [2]IHEP, Beijing

The PANDA detector will be located at the future FAIR facility in Darmstadt. As PANDA has been designed without a global trigger, a large amount of data ($\leq$200 GB/s @ $2 \cdot 10^7$/s interaction rate) has to be distributed and processed in real time. A hardware platform capable of processing this amount of data is the ATCA based Compute Node (CN) developed in close cooperation between IHEP Beijing and our institute. Each node consists of an xTCA carrier board and four AMC/μTCA daughterboards. The carrier board supplies the high bandwidth connectivity between the daugtherboards and the other CNs in the shelf by RocketIO links. In the current prototype design, each AMC board is equipped with a Virtex5FX70T, 4 GB of memory, GBit ethernet and two optical links which allow for high data transfer rate. Beside the event builing, the CNs will run algorithms for cluster finding in the calorimeter data, online tracking and based on these make trigger decisions.

This talk will not only focus on the current hardware and future developments, but also on the setup and performance of our test system, including the status of the algorithm developments.

Supported by BMBF (06GI9107I) und HIC for FAIR.

HK 34.3 Mi 17:30 P 2

Data Transport Challenge at ALICE HLT - Summary and Outlook — •Timo Breitner and Udo Kebschull for the ALICE-Collaboration — Institut für Informatik, Universität Frankfurt, Germany

The ALICE High Level Trigger (HLT) is used for on-line monitoring, filtering, and compression of raw detector data from the ALICE experiment at CERN LHC. A self-developed data-transport framework is used to route the incoming data stream to thousands of different processes distributed on hundreds of computing nodes. Towards the end of 2011, during the Pb-Pb beam period of LHC, we encountered the so-far biggest data challenge while running in compression mode: a large event size, combined with a high luminosity and hence event rate led to an input data rate of up 12 GB/s, and in turn to an output data rate of about 3 GB/s. Future upgrades to LHC and ALICE will lead to even bigger challenges, especially in terms of higher event rates.

The demand for a hardware upgrade at the HLT is obvious, but even more importantly the software has to be made ready for this challenge. The performance of the current software framework in past runs was therefore evaluated and the results shall be presented. Based on the experience of several years of running a new concept shall be proposed, which takes recent and expected future developments in software and hardware technologies into account.

HK 34.4 Mi 17:45 P 2

A Common Read-Out Receiver Card for ALICE DAQ and HLT — •Heiko Engel and Udo Kebschull for the ALICE-Collaboration — IRI, Goethe-Universität Frankfurt

In the ALICE read-out chain, both Data Acquisition (DAQ) and High Level Trigger (HLT) use FPGA-based Read-Out Receiver Cards (RORCs) as interface between the optical Detector Data Link (DDL) and the DAQ and HLT cluster machines. A new version of these cards is currently being developed as a common project of both groups. This new RORC will have a fast PCIe interface, high density parallel optical DDL connections and will combine several of the old cards into one new device. Due to the increased link density and the changed interface to the host machine a completely new read-out architecture has to be connected to the existing software framework. This work includes a custom linux device driver, a scatter-gather based DMA firmware and a software library to interface the new hardware to the existing software framework. All layers can be verified with a custom hardware/software co-simulation environment.

HK 34.5 Mi 18:00 P 2

Der GANDALF 128-Kanal Time-to-Digital Converter — Tobias Baumann, •Maximilian Büchele, Horst Fischer, Matthias Gorzellik, Florian Herrmann, Philipp Jörg, Kay Königsmann, Tobias Kunz, Christoph Michalski, Christian Schill, Sebastian Schopferer und Tobias Szameitat — Physikalisches Institut der Albert-Ludwigs-Universität Freiburg.

Das GANDALF VXS-Modul wurde zur Digitalisierung und Echtzeitanalyse von Detektorsignalen entwickelt. Um die FPGA-Architektur des Mainboards für vielfältige Anwendungen zu erschließen, sind die Signaleingänge auf dedizierten Aufsteckkarten angeordnet. Digitale Aufsteckkarten ermöglichen die Implementierung eines 128-Kanal Time-to-Digital Converters (TDC) in einen Virtex-5 FPGA auf dem GANDALF-Modul. Aufgrund der begrenzten Logikresourcen des FPGAs wird zur Zeitmessung ein Shifted-Clock-Sampling Algorithmus verwendet. Dabei wird das TDC-Register von 16 äquidistant phasenverschobenen Taktsignalen getaktet, die mit zwei PLLs im FPGA generiert werden. Bei dieser Methode muss eine minimale Laufzeitdifferenz des Datensignals zu den 16 Flipflops des TDC-Registers gewährleistet sein. Das Signalrouting kann bei der Implementierung des FPGA-Entwurfs nur indirekt beeinflusst werden. Eine Herausforderung des Projektes liegt daher im homogenen Placement und Routing der Komponenten des TDC-Registers für alle 128 Eingangssignale. Es werden Messungen zur differentiellen und integralen Nichtlinearität sowie der Zeitauflösung von 56 ps des 128-Kanal TDCs vorgestellt. Dieses Projekt wird vom BMBF und EU FP7 unterstützt.

HK 34.6 Mi 18:15 P 2

A Free-Streaming Readout for the CBM Time of Flight wall — •Pierre-Alain Loizeau and Norbert Herrmann for the CBM-Collaboration — Physikalisches Institut der Universität Heidelberg

The Compressed Baryonic Matter (CBM) experiment will be built at the new Facility for Antiproton and Ions Research (FAIR) in Darmstadt, Germany. This fixed target experiment will investigate Heavy Ion collision up to 35 AGeV for Au beams and 89 GeV for protons beams, with high interactions rates: up to 10MHz in Au+Au collision at 25 AGeV. To avoid the limitations of triggered systems at such rates, most CBM detectors will operate a free-streaming readout.

Charged hadrons identification, especially a Kaons-Pions separation up to 3.5 GeV/c, is provided by its Time of Flight wall. This requires a time resolution for the full system in the order of 80ps. The wall is made of MRPC detectors with resistive materials and channel layout adapted to the different rates found in polar angles of 2.5° to 25°. Hit rates up to 200 kHz/channel are expected. Thus electronic with a time resolution of 30 to 40ps, Time over Threshold capability and free-streaming readout is required. This free-streaming mode also require a special care in the synchronization of the system and the data

analysis.

A first prototype of the full high resolution, free-streaming chain was build in Heidelberg, from differential detector to dedicated softwares. It was tested in beam at COSY in Jülich last November, in a hybrid system with triggered systems. It will be described in this contribution and its first in-beam performances will be presented.

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HK 34.7 Mi 18:30 P 2

SPADIC – Self triggered readout ASIC for the CBM transition radiation detectors — Tim Armbruster, Peter Fischer, •Michael Krieger, and Ivan Peric — ZITI, Universität Heidelberg

For the readout of the transition radiation detectors of the planned CBM experiment at FAIR, the self-triggered SPADIC mixed signal ASIC for signal amplification and digitization is under development.

The chip has 32 channels, each composed of a low-noise and low-power charge sensitive amplifier, a 9 bit pipelined ADC running at 25 MHz sampling rate, a programmable digital signal processing unit with 16 bit internal resolution for detector specific tasks such as ion tail cancellation and baseline correction, as well as hit detection logic, which triggers the readout of whole signal snapshots. Data will be sent out in a message-based format through an arbitrated inter-channel network preserving the temporal order of recorded events.

We will show lab and test beam measurements of the available SPADIC prototype chips and present the first version of a full scale chip.

HK 34.8 Mi 18:45 P 2

Comparision of self-triggering front-end electronics for CBM detector prototyping — •Tomas Balog for the CBM-Collaboration — GSI, Darmstadt, Germany — Comenius University, Bratislava, Slovakia

The CBM experiment requires high-rate capable readout electronics. Since the Poisson-distributed collisions of nuclei are not correlated to a global trigger signal, the readout chips as well as the complete data acquisition system must be self-triggered. The n-XYTER chip was developed for neutron experiments and is also used for early prototyping of CBM detectors. The SPADIC chip has been designed for the readout of gaseous detectors of CBM. Their main difference is in the data storing and ordering mechanisms. The n-XYTER chip uses a Token Ring while the SPADIC chip has an ordering FIFO. Simulation studies have been done for both chips in the SystemC hardware description language. In order to achieve a proper comparision, both chips had the same number of channels with the same FIFO depth per channel, and both were simulated at the same bandwidth and hit rates. Resutlts of the simulations are presented including the proper size of the ordering FIFO and a comparision of the performance of both front-end chips.

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