# HK 10: Instrumentation

Zeit: Montag 11:00–13:00 Raum: WIL-A221

HK 10.1 Mo 11:00 WIL-A221

**The CBM Time of Flight wall Free-streaming Readout** — •Pierre-Alain Loizeau and Norbert Herrmann for the CBM-Collaboration — Physikalisches Institut der Universität Heidelberg

The Compressed Baryonic Matter (CBM) experiment is planned to start operating in 2018 at the Facility for Antiproton and Ions Research (FAIR) in Darmstadt, Germany. This fixed target experiment will start taking data with incident beams of 2 to 11 AGeV for Au and up to 29 GeV for protons. Due to the high interaction rate of up to 10MHz, triggered systems would face some limitations and most detectors will have a free-streaming readout. Charged hadrons identification is provided by a Time of Flight wall based on MRPC detectors with a free-streaming readout chain including data reduction and aggregation.

As all input signals need to be transported, the bandwidth between each pair of elements of the readout is important. Studies of input and data rates at different levels were done with realistic detector design.

Two recent hardware developments were made on the digitizer part of the readout chain. A free-streaming mode for the HADES TRB3 board is developed. This allows to use the advantages of FPGA TDC in terms of channels per chip and time resolution. The first iteration of the GET4 TDC chip is also now available and was tested in beam with RPC prototypes in November 2012 at GSI Darmstadt.

Results from this beamtime and later tests will be presented. This includes a comparison between data selection based on a synchronization with a triggered system and selection based on the data themselves.

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HK 10.2 Mo 11:15 WIL-A221

**A Readout System for the PANDA MVD Trapezoidal Silicon Strip Sensors** — •Dariusch Deermann[1], James Ritman[1], Tobias Stockmanns[1], Marius Mertens[1], Simone Esch[1], Robert Schnell[2], Hans-Georg Zaunick[2], and Sebastian Krah[3] for the PANDA-Collaboration — [1]IKP-1, Forschungszentrum Jülich, Wilhelm-Johnen-Straße, 52428 Jülich — [2]II. Physikalisches Institut, Justus-Liebig-Universität Gießen, Heinrich-Buff-Ring 16, 35392 Gießen — [3]Helmholtz-Institut für Strahlen- und Kernphysik, Rheinische Friedrich-Wilhelms-Universität Bonn, Nussallee 14-16, 53115 Bonn

The $\overline{\text{P}}$ANDA-experiment will be one of the main experiments inside the upcoming Facility for Antiproton and Ion Research (FAIR) at the GSI in Darmstadt. The fixed target experiment will explore $\overline{\text{p}}$p annihilation in the charm mass region with intense, phase space cooled beams with momenta between 1.5 and 15 GeV/c.

The innermost subdetector of $\overline{\text{P}}$ANDA will be the Micro Vertex Detector (MVD) and consists of silicon strip and pixel detectors.

In order to operate and test the first trapezoidal strip sensor prototypes of the MVD, a readout system has to be prepared. Therefore a supply board, an ADC-card and sensor board for the trapezoidal strip sensors are necessary to operate the sensors together with the existing Juelich Digital Readout System.

In this talk the adaption of the Juelich Digital Readout System for the trapezoidal silicon strip sensors will be presented.

HK 10.3 Mo 11:30 WIL-A221

**Upgrade of the Juelich Digital Readout System for $\overline{\text{P}}$ANDA development** — •Simone Esch, Marius C. Mertens, Tobias Stockmanns, and James Ritman for the PANDA-Collaboration — IKP Forschungszentrum Jülich

The $\overline{\text{P}}$ANDA detector is one of the main experiments at the upcoming Facility for Antiproton and Ion Research in Darmstadt (FAIR). The fixed target experiment will explore $\overline{\text{p}}$p annihilation with intense, phase space cooled beams with momenta between 1.5 and 15 GeV/c. For the development of the Micro Vertex Detector (MVD), the innermost tracking detector of $\overline{\text{P}}$ANDA, the evaluation of prototypes and detector parts is very important. Different prototypes of the pixel front-end chip ToPix (Torino Pixel) need to be tested and characterized under similar conditions to improve the development. To control these devices under test (DUT) and to save the collected data a suitable readout system is necessary. To have similar conditions for different prototypes a modular concept of a readout system is required which can be adapted in a simple way to the specific interface of different types of electronics. To meet the requirements of an upcoming full size ToPix prototype and online analysis an upgrade of the Juelich Digital Readout System was developed. We will present the concepts and the upgrade of the FPGA based Jülich digital readout system and measurements of the recent MVD pixel front-end prototype ToPix3. First tests of the implementation of the radiation hard GBT transfer protocol are also shown.

HK 10.4 Mo 11:45 WIL-A221

**Electronic Readout for THGEM detectors based on FPGA TDCs** — Tobias Baumann, Maximilian Büchele, Horst Fischer, Matthias Gorzellik, Tobias Grussenmeyer, •Florian Herrmann, Philipp Jörg, Kay Königsmann, Paul Kremser, Tobias Kunz, Christoph Michalski, Sebastian Schopferer, and Tobias Szameitat — Physikalisches Institut der Universität Freiburg for the COMPASS-II RICH upgrade Group

In the framework of the RD51 programme the characteristics of a new detector design, called THGEM, which is based on multi-layer arrangements of printed circuit board material, is investigated. The THGEMs combine the advantages for covering gains up to $10^6$ in electron multiplication at large detector areas and low material budget. Studies are performed by extending the design to a hybrid gas detector by adding a Micromega layer, which significantly improves the ion back flow ratio of the chamber.

With the upgrade of the COMPASS experiment at CERN a MWPC plane of the RICH-1 detector will be replaced by installing THGEM chambers. This summarizes to 40k channels of electronic readout, including amplification, discrimination and time-to-digital conversion of the anode signals. Due to the expected hit rate of the detector we design a cost-efficient TDC, based on Artix7 FPGA technology, with time resolution below 100ps and sufficient hit buffer depth. To cover the large readout area the data is transferred via optical fibres to a central readout system which is part of the GANDALF framework.

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HK 10.5 Mo 12:00 WIL-A221

**The GANDALF 128-channel Time-to-Digital Converter** — Tobias Baumann, •Maximilian Büchele, Horst Fischer, Matthias Gorzellik, Tobias Grussenmeyer, Florian Herrmann, Phillip Jörg, Paul Kremser, Tobias Kunz, Christoph Michalski, Sebastian Schopferer, and Tobias Szameitat — Physikalisches Institut der Albert-Ludwigs-Universität Freiburg

In particle physics experiments, Time-to-Digital Converters (TDC) perform accurate time measurements, thus to allow for charged particle identification and tracking. We have developed within the GANDALF framework a 128-channel TDC, implemented in a Xilinx Virtex-5 FPGA. A time resolution better than 93 ps has been verified for all channels. In contrast to previous FPGA-based TDC, the design makes use of a shifted clock sampling algorithm. In this concept, the input signal is sampled with flip-flops driven by a set of equidistant phase-shifted clocks. The TDC register length depends only on the number of phase-shifted clocks and therefore permits to process a large number of channels in a very resource-efficient way.

As not only time measurements but also simultaneous rate measurements are required for many applications, we present a combination of 96 scaler and TDC channels implemented in the same FPGA on the GANDALF 6U-VME64x/VXS carrier board. In addition to the experiment trigger, an internal generated pseudo-random trigger is applied in order to produce two independent data streams. This may allow for online monitoring of the detector device. This project is supported by BMBF and EU FP7 (Grant Agreement 283286).

HK 10.6 Mo 12:15 WIL-A221

**Performance of the HADES DAQ in Au+Au** — •Jan Michel for the HADES-Collaboration — Goethe-Universität, Frankfurt

The High Acceptance DiElectron Spectrometer (HADES) is located at the SIS-18 accelerator at the GSI Helmholtz Center for Heavy Ion Research in Darmstadt. In April 2012 a five-week experimental run using a 1.23 AGeV gold beam focused on a 15-fold segmented gold target was conducted.

One major reason for this successful data taking was the upgraded data acquisition system. An optical network running a customized network protocol (TrbNet) connects the frontend modules with read-out nodes. Here the data stream is converted to Gigabit Ethernet packets

which are subsequently transported to a server farm using commodity hardware. All electronic components are supervised using a new, web-based monitoring system making use of the inherent slow-control features of TrbNet. In total, the system comprises of 550 FPGA-based modules, 30 Gigabit Ethernet links, four multi-core servers and 150 TB of local disk storage. The whole system is able to record event data in heavy-ion collissions at rates of up to 30 kHz and 800 MByte/s. During the experiment, the mean rates were 8 kHz and 150 MByte/s respectively mainly due to detector constraints. As a result, $7.7 \cdot 10^9$ events with a total volume of 140 TB were recorded throughout the run. In this contribution the set-up, performance figures and the slow-control concept will be shown.

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HK 10.7 Mo 12:30 WIL-A221

**Design concepts and measurements of the CBM DAQ network** — •Frank Lemke and Sven Schatral for the CBM-Collaboration — Universität Heidelberg

In the context of the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt a hierarchical structured data acquisition (DAQ) network is used to readout particle detectors over synchronized bidirectional links. Interconnects operate with unified connections using one special protocol (CBMnet) in the whole readout. Thereby no protocol conversion is required. Communication modules provided for various hardware devices are easy to insert into new ASICs or FPGAs. Thus, more and more devices can be equipped with these modules. This saves design time and enables usage of existing structures optimized for CBM requirements. Besides multiple supported FPGA platforms, the first front-end ASIC, the SPADIC, was developed and it has been completely tested. A second front-end detector ASIC with CBMnet, the STSXYTER, was submitted at the end of October, expanding the usage of CBMnet to further readout chains. Unbalanced line handling enables higher data rates with reduced wiring overhead. The current implemented universal readout controller board using a Spartan 6 FPGA offers the ability to synchronize and readout up to four front-end boards. The synchronization mechanism based on deterministic and simultaneous arrival of deterministic latency messages (DLM) in all front-end devices works with accuracy better than 2ns. Not only the synchronization, but also all other communication classes have been tested successfully.

HK 10.8 Mo 12:45 WIL-A221

**Technical commissioning of AGATA at GSI: coupling of the DAQ*** — •Damian Ralet[1], Stephane Pietri[2], Hakan Johansson[3], Dino Balzzacco[4], Xavier Grave[5], Nikolaus Kurz[2], Yann Aubert[5], Nicolas Dosme[5], Amel Korichi[5], Eric Legay[5], Juergen Gerl[2], and Norbert Pietralla[1] for the AGATA-Collaboration — [1]Institut für Kernphysik, Technische Universität Darmstadt, Darmstadt, Germany — [2]GSI Helmholtzzentrum für Scherionenforschung GmbH, Darmstadt, Germany — [3]Chalmers University of Technology, Göteborg, Sweden — [4]Istituto Nazionale di Fisica Nucleare Sezione di Padova, Padova, Italy — [5]CSNSM Université Paris-Sud, Orsay, France

The PRESPEC experiment for high-resolution gamma-ray spectroscopy using radioactive ion beams at the FRagment Separator of GSI together with the LYCCA-1 calorimeter and the AGATA [1] detector array has been commissioned early 2012. Main goals of the commissioning were to test the new trigger logic using FPGA-based modules and to test the coupling of the two data acquisition systems, NARVAL for the AGATA detectors, and MBS for the FRS+LYCCA detectors. The performance of the DAQ coupling will be presented and various trigger configurations for background suppression will be discussed.

[1] AGATA–Advanced GAmma Tracking Array, Nucl. Instr. Meth. A 668, 26 (2012)

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