HK 6: Instrumentierung

Zeit: Montag 14:00–15:30 Raum: HZ 8

HK 6.1 Mo 14:00 HZ 8

TDC for the front end architecture in the PANDA MVD — •Alberto Riccardi[1], Kai Thomas Brinkmann[1], Valentino Di Pietro[1], Sara Garbolino[2], Angelo Rivetti[2], and Manuel Rolo[2] for the PANDA-Collaboration — [1]II Physikalisches Institut Justus-Liebig-Universität Giessen, Giessen, Germany — [2]INFN Sezione di Torino, Torino, Italy

In nuclear detectors the information on the energy of the particle is usually obtained by measuring the amplitude of the signal delivered by the sensor. The low voltage power supply used in modern deep submicron technologies constrains the maximum dynamic range of the ADC. So we can obtain the energy information with time-based techniques, in which the energy is associated with the duration of the signal through the Time over Threshold method. This work is focused on the PANDA Micro Vertex Detector and explores the possibility of applying a time-based readout approach for the microstrip sensors. In PANDA , the strip system must cope with hit rates up to 50 kHz per channel. Therefore, the front-end output must be relatively short. This implies that the clock resolution is not enough to measure the signal duration, so it is necessary to use a Time to Digital Converter. The front-end and the TDC structure are designed in a 0.11um CMOS process. The TDC chosen is based on an analog clock interpolator because it combines good time resolution with a fairly simple implementation and low power consumption. In the presentation the architectures with their will be described and the challenges associated to its implementation discussed. Supported by BMBF, HGS-HIRe and JCHP.

HK 6.2 Mo 14:15 HZ 8

TRB3-based DAQ systems - A collaborative approach — •Jan Michel for the TRB3-Collaboration — Goethe-Universität Frankfurt

Modern detector systems have become complex and the demands on data- and event-rates made designing a fitting data acquisition scheme a major task. On the other hand, many small research groups need a fast way to set up a small system for testing of detector prototypes.

During the past years, the data acquisition system of the HADES detector at GSI has been upgraded. Within this project, a huge set of electronic components, a network data transport protocol and software for data storage as well as control and monitoring of the detector were developed. This framework has been further extended, a new versatile FPGA platform (TRB3) has been built and can be adapted to many different needs by AddOn and front-end modules.

The full toolchain has been successfully used by various sub-groups of the FAIR experiments CBM, PANDA and HADES. Several other detector groups are interested in the project and are actively contributing. This talk will focus on the advantages such a collaborative community has for all partners. Among these is the small amount of work to be contributed by the individual, the fast installation time of new set-ups and the versatile software environment to which all users contribute.

This work has been supported by BMBF, HIC for FAIR, and GSI.

HK 6.3 Mo 14:30 HZ 8

Upgrade of the Data Acquisition System for the A2 Experiment at MAMI — •Andreas Neiser and Wolfgang Gradl for the TRB3-Collaboration — Institut für Kernphysik, Johann-Joachim-Becher-Weg 45, Mainz

The A2 collaboration at the electron accelarator MAMI in Mainz uses energy-tagged photons to produce light mesons off the nucleon. Its current data acquisition system is the major performance bottleneck under typical trigger conditions. Furthermore, the availability of spare parts is limited, which renders the maintainability for the next decade difficult. Thus, an upgraded system is desirable for A2 to achieve the upcoming experimental goals. For this upgrade, an FPGA-based solution using the TRB3 is being considered.

The TRB3 is a multi-purpose $4+1$ FPGA board and implements a $4 \times 65 + 4 = 264$ channel time-to-digital converter (TDC) with 11 ps RMS precision between two channels. It was developed at GSI in Darmstadt including different front-ends for signal discrimination and charge measurements. For the precursor TRB2, a charge-to-digital precision of 0.2 % was shown. Owing to its flexible design, it is an attractive upgrade option for A2.

We present the successful integration of the TRB3 into the existing A2 data acquisition system at the trigger and the data read-out interface. First test measurements at our 4π NaI calorimeter Crystal Ball with up to 16 channels yielded promising results. The performance of the TRB3 platform seems to be sufficient for the future requirements of A2. An outlook on upscaling and deploying the system is given.

HK 6.4 Mo 14:45 HZ 8

Frontend Electronics for high-precision single photo-electron timing using FPGA-TDCs — •Matteo Cardinali for the PANDA Cherenkov-Collaboration — Helmholtz Institut Mainz

The next generation of high-luminosity experiments requires excellent Particle Identification (PID) detectors which calls for Imaging Cherenkov counters with fast electronics to cope with the expected data rates. The planned PANDA experiment at FAIR expects average interaction rates of 20MHz. A Barrel DIRC will provide PID in the central region of the Target Spectrometer. A single photo-electron timing resolution of better than 100ps is projected for the Barrel DIRC to disentangle the complicated patterns created by the focusing optics on the image plane. The typically large amount of readout channels (approx 15,000 in case of the PANDA Barrel DIRC) places non-negligible limits on size and power consumption of the Front-End Electronics (FEE). The proposed design is based on the TRBv3 readout using FPGA-TDCs with a precision better than 20ps RMS and custom FEE with high-bandwidth pre-amplifiers and fast discriminators. Two types of FEE cards optimised for reading out 64-channel Photonis Planacon MCP-PMTs were tested: one based on the NINO ASIC developed for the ALICE RPC readout and the other, called PaDiWa, using FPGA-based discriminators. Both types of FEE cards were tested with a small DIRC prototype comprising a radiator bar with focusing lens and an oil-filled expansion volume instrumented with 6 Planacon 64-channel MCP-PMTs. In the presentation the result of a test experiment performed at MAMI B, Mainz, will be addressed.

HK 6.5 Mo 15:00 HZ 8

Development of a digital trigger system to identify recoil protons at COMPASS-II — Maximilian Büchele, Horst Fischer, •Matthias Gorzellik, Tobias Grussenmeyer, Florian Herrmann, Philipp Jörg, Kay Königsmann, Paul Kremser, and Sebastian Schopferer — Albert-Ludwigs-Universität Freiburg

The GANDALF framework has been developed to deliver a high precision, high performance detector readout and trigger system for particle physics experiments such as the COMPASS-II experiment at CERN. Combining the high performance pulse digitization and feature extraction capabilities of twelve GANDALF modules, each comprising a Virtex-5 SX95T, with the strong computation power of a Virtex-6 SX315T FGPA operated on the TIGER module, we present a digital trigger system for a recoil proton detector.

The trigger system was setup and commissioned successfully during a data taking period in 2012. It was mainly used for the calibration of the recoil proton detector and in tagging mode to identify proton tracks online.

Supported by BMBF and EU FP7 (Grant Agreement 283286).

HK 6.6 Mo 15:15 HZ 8

Self-triggering readout system for the neutron lifetime experiment PENeLOPE — •Dominik Steffen for the PENeLOPE-Collaboration — Technische Universität München

Modern experiments permanently improve the precision of parameters in nuclear and particle physics. Besides high-performance detectors, state-of-the-art readout electronis and recent data acqusition systems contribute substantially to the increasingly better accuracy. This talk will therefore present the readout system, which is being designed for the neutron lifetime experiment PENeLOPE, currently under construction at Technische Universität München.

The system*s readout chain involves preamplifier, shaper, sampling ADC, and a data processing stage implemented on field programmable gate arrays (FPGAs). The FPGAs perform the task of online data analysis and formatting and are able to transfer data to a computer via a high-speed Ethernet connection. An advanced algorithm enables them to calculate the pedestal for every single channel online, and to reliably detect all signals above noise. Due to this incorporated signal detection, the triggerless system is able to process and to format pulse

shapes from around 1,000 channels simultaneously, each of which is hit by 10 particles/sec. This corresponds to a data rate of 1.5 MB/sec, which is read out to a computer where the pulse shapes are available for further analysis. In the talk, performance and first tests of this readout system will be presented in detail.