HK 59: Instrumentation 17

Time: Thursday 17:00–19:00 Location: M/HS1

Group Report HK 59.1 Thu 17:00 M/HS1

Results of the first Tests Measurements using the Prototype Trigger-Less Data Acquisition for the $\overline{\text{P}}$ANDA Experiment — •Milan Wagner, Thomas Gessler, Wolfgang Kühn, Sören Lange, Björn Spruck, and Marcel Werner for the PANDA-Collaboration — JLU Gießen

The $\overline{\text{P}}$ANDA detector will be a located at the high energy storage ring (HESR), at the facility for anti protons and ion research (FAIR) in Darmstadt, Germany. It will operate with a very high average interaction rate of about 20 MHz, in a free streaming mode without hardware trigger. Instead of triggering, data filtering will be performed by complete online event reconstruction with a highly parallelized farm of FPGAs as first level and on a farm of GPUs or PCs as a second level. The requirement is a background reduction by a factor of >1000. Parts of the $\overline{\text{P}}$ANDA detector will be pre-assembled and tested at the Forschungszentrum Jülich, before being transported to GSI at a later stage. A prototype trigger-less data acquisition (PTDAQ) will be used during this phase. The main component of the PTDAQ is the Compute Nodes (CN), a xTCA-compliant board based on a Virtex-5 FX70T FPGA, with a μTCA-formfactor. Synchronization is done via a Synchronization Of Data Acquisition (SODA) source. Parts of the functionality were tested in a setup using a 210 MeV electrons beam with a rate of 1 MHz at the Mainz Microtron. In this contribution, we present the first results of test measurements using the PTDAQ system. This work is supported by BMBF(05P12RGFPF), HGS-HIRe for FAIR and the LOEWE-Zentrum HICforFAIR.

HK 59.2 Thu 17:30 M/HS1

The Next Generation CBM MVD Front-end Electronics — •Michael Wiebusch, Jan Michel, Philipp Klaus, and Joachim Stroth for the CBM-MVD-Collaboration — Goethe-Universität, Frankfurt

The Micro Vertex Detector (MVD) for the CBM experiment is a highly granular precision tracking device. Due to the ambitious requirements regarding spatial resolution, radiation hardness, read-out speed and material budget, monolithic active pixel sensors (MAPS) are the most suited detector technology for this purpose. A full read-out chain for these sensors was designed and prototyped, comprising a multi-purpose FPGA platform and specialized front-end electronics. During the last year an updated version of the front-end electronics was produced and successfully commissioned. The current front-end electronics incorporate additional configuration and monitoring capabilities which shall be used to optimize the concept of biasing and routing critical analog signals to the sensor. Tests regarding these issues are ongoing. Recent efforts aim at building a quarter of an MVD station with more than a dozen individual MAPS sensors. This requires the adaption of the front-end electronics to the spacial constraints of the set-up. Also the schematics have to be streamlined based on the insights from the abovementioned tests. This contribution will present the outcomes of the adaption and optimization procedures. *This work has been supported by BMBF (05P12RFFC7), GSI and HIC for FAIR.

HK 59.3 Thu 17:45 M/HS1

A flexible COME and KISS QDC and TDC Read-out Scheme for PMT, MAPD and Diamond Detector Applications — •Adrian Rost for the HADES-Collaboration — Technische Universität Darmstadt, Darmstadt

A flexible COME & KISS Charge-to-Digital-Converter (QDC) and Time-to-Digital-Converter (TDC) read-out scheme will be presented which can be used in a wide range of read-out applications in high energy physics experiments. The focus is on a calorimeter detector read-out via photomultiplier tubes (PMTs) or via multi-pixel avalanche photo-diodes (MAPDs), as well as on diamond detectors for the HADES and CBM experiments at the future FAIR facility in Darmstadt.

The detector input signals are integrated with the help of simple analogue electronics (KISS: **K**eep **i**t **S**mall and **S**imple). Afterwards the charge measurement is transformed into a Time-over-Threshold (ToT) measurement using an commercial (COME: Use **Com**mercial **E**lements) FPGA as a discriminator. The well-established TRBv3 platform will provide a precise FPGA TDC for a ToT measurement of the discriminated signals.

An 8-channel prototype board PaDiWa-AMPS was manufactured and successfully tested in the laboratory and under beam conditions. In this contribution the current status of the read-out concept will be shown.

This work has been supported by VH-NG-823, Helmholtz Alliance HA216/EMMI and GSI.

HK 59.4 Thu 18:00 M/HS1

Overview of DAQ developments for the CBM experiment — •David Emschermann for the CBM-Collaboration — GSI Helmholtzzentrum für Schwerionenforschung GmbH

The Compressed Baryonic Matter experiment (CBM) at the future Facility for Antiproton and Ion Research (FAIR) is a a fixed-target setup operating at very high interaction rates up to 10 MHz. The high rate capability can be achieved with fast and radiation hard detectors equipped with free-streaming readout electronics. A high-speed data acquisition (DAQ) system will forward data volumes of up to 1 TB/s from the CBM cave to the first level event selector (FLES), located 400 m apart. This presentation will showcase recent developments of DAQ components for CBM. We will highlight the anticipated DAQ setup for beam tests scheduled for the end of 2015.

HK 59.5 Thu 18:15 M/HS1

A viable on-chip FPGA configuration memory scrubbing approach for CBM-ToF — •Andrei-Dumitru Oancea, Christian Stüllein, Sebastian Manz, Jano Gebelein, and Udo Kebschull for the CBM-Collaboration — Infrastruktur und Rechnersysteme in der Informationsverarbeitung (IRI), Goethe-Universität, Senckenberganlage 31, 60325 Frankfurt am Main

The ToF Detector of the CBM Experiment will be equipped with FPGA-based read-out boards (ROBs). These ROBs will be operated in a radiation environment, and therefore need a mitigation mechanism against soft errors in the SRAM-based configuration memories of the FPGAs.

The proposed approach combines intrinsic on-chip single upset correction with extrinsic selective frame scrubbing for multiple-bit upsets. The slow control is realized using the GBT-SCA, which is capable of handling interrupts. This enables the new approach of event-driven configuration frame correction. While conventional blind scrubbing leads to a continuous load on the control path, the selective frame scrubbing reduces this load to a minimum.

For verification purposes, radiation tests with a proton beam were performed at COSY, Juelich. The occurred soft errors were classified into single and multiple- bit upsets, enabling an estimation of the rate at which extrinsic intervention is necessary.

HK 59.6 Thu 18:30 M/HS1

Design and prototyping of a readout aggregation ASIC — Frank Lemke[1], •Sven Schatral[1], Indranil Som[2], Tarun Bhattacharyya[2], and Ulrich Bruening[1] for the CBM-Collaboration — [1]ZITI, Universitaet Heidelberg — [2]Indian Institute of Technology Kharagpur

In close collaboration between the Indian Institute of Technology Kharagpur (IITKGP) and the Institute for Computer Engineering (ZITI) at the University of Heidelberg a readout aggregation ASIC was designed. This happened in the context of the Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR). The ASIC is designed in 65nm TSMC technology. Its miniASIC tapeout to verify the analog and high-speed components is scheduled to the first quarter of 2015. This mixed-signal ASIC consists of a full-custom 5Gb/s serializer/deserializer, designed by the IITKGP including design elements such as phase-locked loop, bandgap reference, and clock data recovery, and a digital designed network communication and aggregation part designed by the ZITI. In addition, there are test structures and an I2C readout integrated to ease bring up and monitoring. A specialty of this test ASIC is the aggregation of links featuring different data rates, running with bundles of 500 MB/s LVDS. This enables flexible readout setups of mixed detectors respectively readout of various chips. As communication protocol, a unified link protocol is used including control messages, data messages, and synchronization messages on an identical lane. The design has been simulated, verified, and hardware emulated using Spartan 6 FPGAs.

HK 59.7 Thu 18:45 M/HS1

LAND/R3B DAQ developments — •Hans Törnqvist[1], Thomas Aumann[1], Haik Simon[2], Håkan Johansson[3], and Bastian Löher[1] for the R3B-Collaboration — [1]Technische Universität Darmstadt, Darmstadt, Germany — [2]GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany — [3]Chalmers Institute of Technology, Göteborg, Sweden

Existing experimental setups aim to exploit most of the improved capabilities and specifications of the upcoming FAIR facility at GSI. Their DAQ designs will require some re-evaluation and upgrades. This presentation summarizes the R3B experimental campaigns in 2014, where the R3B DAQ was subject to testing of several new features that will aid researchers in using larger and more complicated experimental setups in the future. It also acted as part of a small testing ground for the NUSTAR DAQ infrastructure. In order to allow to extract correlations between several experimental sites, new suggested triggering and timestamping implementations were tested over significant distances. Also, with growing experimental complexity comes a greater risk of problems that may be difficult to characterize and solve. To this end, essential remote monitoring and debugging tools have been used successfully.