HK 29: Instrumentation VII

Zeit: Dienstag 16:30–18:15 Raum: S1/01 A2

HK 29.1 Di 16:30 S1/01 A2

FPGA helix tracking algorithm for PANDA — •Yutie Liang[1], Martin Galuska[1], Thomas Gessler[1], Wolfgang Kühn[1], Jens Sören Lange[1], David Münchow[1], and Hua Ye[2] for the PANDA-Collaboration — [1]II. Physikalisches Institut, University of Giessen — [2]Institute of High Energy Physics, CAS, China

The PANDA detector is a general-purpose detector for physics with high luminosity cooled antiproton beams, planed to operate at the FAIR facility in Darmstadt, Germany. The central detector includes a silicon Micro Vertex Detector (MVD) and a Straw Tube Tracker (STT). Without any hardware trigger, large amounts of raw data are streaming into the data acquisition system. The data reduction task is performed in the online system by reconstruction algorithms programmed on FPGAs (Field Programmable Gate Arrays) as first level and on a farm of GPUs or PCs as a second level. One important part in the system is the online track reconstruction. In this presentation, an online tracking algorithm for helix tracking reconstruction in the solenoidal field is shown. The VHDL-based algorithm is tested with different types of events, at different event rate. Furthermore, a study of T0 extraction from the tracking algorithm is performed. A concept of simultaneous tracking and T0 determination is presented.

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HK 29.2 Di 16:45 S1/01 A2

The Prototype Triggerless Data Aquisition of the PANDA Experiment — •Milan Wagner, Simon Reiter, Sören Lange, and Wolfgang Kühn for the PANDA-Collaboration — II. Physikalisches Institut

The PANDA detector will operate with a very high interaction rate of up to 20 MHz, in a free streaming mode without hardware trigger. Data filtering will be performed by complete online event reconstruction with a highly parallelized farm of FPGAs as first level and on a farm of GPUs or PCs as a second level. The requirement is a back- ground reduction by a factor of >1000. A prototype trigger-less data acquisition (PTDAQ) system for the detector validation measurements comprises free streaming and synchronization readout, for event building and filtering has been developed. A first in beam environment test was performed at the Mainzer Mikrotron, reading out the barrel electromagnetic calorimeter prototype (Proto120). *This work is supported by BMBF(05P12RGFPF), HGS-HIRe for FAIR and the LOEWE-Zentrum HIGforFAIR.

HK 29.3 Di 17:00 S1/01 A2

A test system for electronics components of the PANDA MVD. — •Alessandra Lai, Tobias Stockmanns, and James Ritman for the PANDA-Collaboration — Forschungszentrum Juelich

The PANDA experiment is one of the main devices at the upcoming Facility for Antiproton and Ion Research(FAIR), under construction in Darmstadt, Germany. This fixed target experiment will study the transition region between perturbative and non-perturbative QCD in the energy regime of the charmonium. The innermost sub-detector system of the target spectrometer of the PANDA experiment is the Micro Vertex Detector(MVD). Two types of silicon detectors will be used: pixel detectors and double-sided strip detectors. Two front-end chips are required: the Torino Pixel ASIC(ToPix) and the PANDA Strip ASIC(PASTA). Both are designed to transmit data at a rate of several hundred Megabits per second and are capable of handling the expected hit rate in hot spots of the detector. One key component in the development of new front-end electronics is a test system capable to handle these high rates. It should be flexible enough to test different kinds of front-end electronics and it should be easy to adapt to new prototypes. Therefore, an FPGA-based system is the ideal candidate. For this test system suitable firmware and a software framework are needed. Such a system is under development at the Forschungszentrum Jülich. The main component of the Jülich Digital Readout System(JDRS) is a Virtex 6 FPGA on a development board from Xilinx.

In this talk, the mentioned read-out system will be introduced and lab tests with the front-end electronics of the MVD will be presented.

HK 29.4 Di 17:15 S1/01 A2

Evaluation of a feature extraction framework for FPGA firmware generation during a beam-test at CERN-SPS for the CBM-TRD experiment — •Cruz de Jesus Garcia Chavez, Carlos Enrique Munoz Castillo, and Udo Kebschull for the CBM-Collaboration — Infrastructure and Computer Systems in Data Processing (IRI), Goethe University, Frankfurt am Main, Germany

A feature extraction framework has been developed to allow easy FPGA firmware generation for specific feature extraction algorithms in order to find and extract regions of interest within time-based signals. This framework allows the instantiation of multiple well-known feature extraction algorithms such as center of gravity, time over threshold and cluster finder, just to mention a few of them. A graphical user interface has also been built on top of the framework to provide a user-friendly way to visualize the data-flow architecture across processing stages. The FPGA platform constraints are automatically set up by the framework itself. This feature reduces the need of low-level hardware configuration knowledge that would normally be provided by the user, centering the attention in setting up the processing algorithms for the given task more than in writing hardware description code.

During November 2015, a beam-test was performed at the CERN-SPS hall. The presented framework was used to generate a firmware for the SysCore3 FPGA development board used to readout two TRD detectors by means of the SPADIC 1.0 front-end chip. The framework architecture, design methodology, as well as the achieved results during the mentioned beam-test will be presented.

HK 29.5 Di 17:30 S1/01 A2

Overview and Future Developments of the FPGA–based DAQ of COMPASS — Yunpeng Bai[1], Martin Bodlak[2], Vladimir Frolov[3], Vladimir Jary[4], Stefan Huber[1], Igor Konorov[1], Dmytro Levit[1], Josef Novy[3,4], •Dominik Steffen[1,3], and Miroslav Virius[4] — [1]Physik-Department E18, Technische Universität München — [2]Department of Low-Temperature Physics, Charles University Prague — [3]European Organization for Nuclear Research - CERN — [4]Faculty of Nuclear Sciences and Physical Engineering, Czech Technical University

COMPASS is a fixed–target experiment at the SPS accelerator at CERN dedicated to the study of hadron structure and spectroscopy. In 2014, an FPGA–based data acquisition system (FDAQ) was deployed. Its hardware event builder consisting of nine custom designed FPGA–cards replaced 30 distributed online computers and around 100 PCI cards. As a result, the new DAQ provides higher bandwidth and better reliability. By buffering the data, the system exploits the spill structure of the SPS averaging the maximum on–spill data rate of 1.5 GB/s over the whole SPS duty cycle. A modern run control software allows user–friendly monitoring and configuration of the hardware nodes of the event builder. From 2016, it is planned to wire all point–to–point high–speed links via a fully programmable crosspoint switch. The crosspoint switch will provide a fully customizable DAQ network topology between front–end electronics, the event building hardware, and the readout computers. It will therefore simplify compensation for hardware failure and improve load balancing.

HK 29.6 Di 17:45 S1/01 A2

Data acquisition at the BGO-OD experiment — •Daniel Hammann for the BGO-OD-Collaboration — Physikalisches Institut, Universität Bonn

The BGO-OD experiment, located at the 3.5 GeV electron accelerator ELSA in Bonn, is investigating photo-production of mesons. It combines a highly segmented electromagnetic calorimeter, covering almost 4π, with an open dipole spectrometer for the forward angles. To acquire the data from the various detectors of the setup, a distributed data acquisition system was set up. A global trigger signal is distributed using a dedicated FPGA based synchronization system. This trigger signal is also used as hardware reference for all time measurements. Offline reconstruction of the trigger logic allows to further improve the time reference in software. An even more precise timing reference can be derived from the ELSA acceleration frequency. A dedicated TDC measures the phase difference between the global trigger signal and the ELSA frequency. With this the knowledge of the event time is only limited by the intrinsic resolution of the TDC and the electron bunch length.

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HK 29.7 Di 18:00 S1/01 A2

The CBM-STS front-end electronics — •Adrian Rodriguez Rodriguez for the CBM-Collaboration — GSI Helmholtzzentrum fur Schwerionenforschung GmbH

The Silicon Tracking System (STS) of the CBM experiment is based on double-sided silicon microstrip sensors, arranged in 8 tracking stations. It poses the most demanding requirements in terms of readout rates and electronics density of all CBM detectors. The STS-XYTER is a 128 channel, low power, self triggering ASIC which provides timing and energy information for each hit sensor strip. One of the main goals on the chip design is to achieve a low level noise performance (below 1000 e^- rms). The first version of the chip has been tested and characterized in prototype front-end board. The second version of the ASIC is under revision to be submitted in early 2016. An overview of main tests outcomes and an outlook on version 2 will be presented.

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