T 42: Trigger und DAQ II

Zeit: Montag 16:45–18:45 Raum: VMP11 HS

T 42.1 Mo 16:45 VMP11 HS

The Data Handling Processor of the Belle II DEPFET Detector — •Leonard Germic, Tomasz Hemperek, Tetsuichi Kishishita, Botho Paschen, Florian Lütticke, Hans Krüger, Carlos Marinas, and Norbert Wermes for the Belle II-Collaboration — Universität Bonn

A two layer highly granular DEPFET pixel detector will be operated as the innermost subsystem of the Belle II experiment, at the new Japanese super flavor factory (SuperKEKB). Such a finely segmented system will allow to improve the vertex reconstruction in such ultra high luminosity environment but, at the same time, the raw data stream generated by the 8 million pixel detector will exceed the capability of real-time processing due to its high frame rate, considering the limited material budged and strict space constrains. For this reason a new ASIC, the Data Handling Processor (DHP) is designed to provide data processing at the level of the front-end electronics, such as zero-suppression and common mode correction. Additional feature of the Data Handling Processor is the control block, providing control signals for the on-module ASICs used in the pixel detector. In this contribution, the description of the latest chip revision in TSMC 65 nm technology together with the latest test results of the interface functionality tests are presented.

T 42.2 Mo 17:00 VMP11 HS

Test Runs of a Belle II PXD Prototype Readout System — •Dennis Getzkow[1], Thomas Gessler[2], Wolfgang Kühn[1], Sören Lange[1], and Klemens Lautenbach[1] for the Belle II-Collaboration — [1]Justus-Liebig-Universität Gießen, II. Physikalisches Institut — [2]KEK, Tsukuba (Japan)

The Belle II PXD readout system (called ONSEN for Online Selection Nodes) uses ATCA (Advanced Telecommunications Architecture) boards with Xilinx Virtex-5 FX70T FPGAs and high speed optical links (6.5 Gbit/s each). The full system consists of 9 carrier boards and 33 daughter cards. The ONSEN system has several interfaces: (a) it receives PXD data from the DHH (Data Handling Hybrid) system, (b) it receives ROI (Regions-of-Interest) data for online data reduction from the HLT (High Level Trigger) system by GbE, and (c) it features data ports to two event builders: EVB1 combines data from all detectors except PXD (in order to generate the ROIs) and EVB2 combines the reduced PXD data with all other data. One of the critical issues is the matching of trigger numbers in the data (received by DHH from the timing distribution system) and trigger numbers in the ROIs (received by the HLT). In order to test the interfaces, in particular for a high HLT rate up to 30 kHz, a prototype system with 3 daughter cards was installed at KEK and tested with DHH, HLT and EVB2. Test results will be presented.

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T 42.3 Mo 17:15 VMP11 HS

First considerations for a readout system for the ILD TPC with the Timepix3 — •Tobias Schiffer for the LCTPC-Deutschland-Collaboration — Universität Bonn

For the planned International Linear Collider (ILC) two detectors are proposed. One of them, the International Large Detector (ILD) uses a Time Projektion Chamber (TPC) as the main tracking device. As a readout system for this TPC, pixel chips are one of the considered options. An integrated Micromegas stage is foreseen as gas amplification stage, which is built directly on top of the chip.

Since first tests of a Pixel-TPC with 160 Timepix ASICs showed promising results, one is interested in developing a detector using the Timepix3 ASIC. It has several advantages, first of all its feature to measure ToT and a ToA at the same time and its significantly increased readout rate.

For this purpose a readout system needs to be developed which fulfils the requirements of the Timpix3 ASIC and also has a high scalability. The main challenges are the high speed readout with a clock of up to 640 MHz and the reliability of the system. Also, the data driven as well as the frame-based readout of the Timepix3 needs to be considered for the implementation. The main goal is to provide a fast and parallel readout of several million channels.

An overview and the status of the planning will be given. Also, the development challenges will be discussed.

T 42.4 Mo 17:30 VMP11 HS

The DATCON System of the Belle II Experiment - Tracking and Data Reduction — •Christian Wessel, Jochen Dingfelder, Carlos Marinas, and Bruno Deschamps — Universität Bonn - Physikalisches Institut

The SuperKEKB e^+e^- accelerator at KEK in Japan will have a luminosity which is a factor of 40 higher than the luminosity of its predecessor KEKB. The Belle II detector at SuperKEKB will contain a two-layer pixel detector at radii of 1.421 and 2.179 cm from the interaction point, based on the DEPFET (DEpleted P-channel Field Effect Transistor) technology. It is surrounded by four layers of strip detectors. Due to the high collision rate, the data rate of the pixel detector needs to by drastically reduced by an online data reduction system. The DATCON (Data Acquisition Tracking and Concentrator Online Node) system performs track reconstruction in the SVD (Strip Vertex Detector) and extrapolates to the PXD (PiXel Detector) to calculate ROI and to keep only hits in the ROI. The track reconstruction algorithm is based on a Hough transform, which reduces track finding to finding intersection points in the Hough parameter space. In this talk the employed algorithm for fast online track reconstruction on FPGA, ROI finding and the performance of the data reduction are presented.

T 42.5 Mo 17:45 VMP11 HS

Online Track and Vertex Reconstruction on GPUs for the Mu3e Experiment — •Dorothea vom Bruch for the Mu3e-Collaboration — Institut für Kernphysik, Johannes Gutenberg-Universität Mainz

The Mu3e experiment searches for the lepton flavour violating decay $\mu \to eee$, aiming at a branching ratio sensitivity better than 10^{-16}.To reach this sensitivity, muon rates above 10^9 μ/s are required. A high precision silicon tracking detector combined with excellent timing resolution from scintillating fibers and tiles will measure the momenta, vertices and timing of the decay products of muons stopped in the target to suppress background.

The trigger-less readout system will deliver about 100 GB/s of zero-suppressed data. A network of optical links and switching FPGAs sends the complete detector data for a time slice to one node of the filter farm. An FPGA inside the filter farm PC transfers the event data to the GPU via PCIe direct memory access. The GPU finds and fits tracks using a 3D tracking algorithm for multiple scattering dominated resolution. In a second step, a three track vertex fit is performed, allowing for a reduction of the output data rate to below 100 MB/s by removing combinatorial background. The talk discusses the data flow from the FPGA to the GPU as well as the implementation and performance of the track and vertex fits on the GPU.

T 42.6 Mo 18:00 VMP11 HS

GPU-based online track reconstruction for the MuPix-telescope — •Carsten Grzesik for the Mu3e-Collaboration — JGU, Mainz

The MuPix telescope is a beam telescope consisting of High Voltage Monolithic Active Pixel Sensors (HV-MAPS). This type of sensor is going to be used for the Mu3e experiment, which is aiming to measure the lepton flavor violating decay $\mu \to eee$ with an ultimate sensitivity of 10^{-16}. This sensitivity requires a high muon decay rate in the order of 1 GHz leading to a data rate of about 1 TBit/s for the whole detector. This needs to be reduced by a factor 1000 using online event selection algorithms on Graphical Processing Units (GPUs) before passing the data to the storage.

A test setup for the MuPix sensors and parts of the Mu3e tracking detector readout is realized in a four plane telescope. The telescope can also be used to show the usability of an online track reconstruction using GPUs. As a result the telescope can provide online information about efficiencies of a device under test or the alignment of the telescope itself. This talk discusses the implementation of the GPU based track reconstruction and shows some results from recent testbeam campaigns.

T 42.7 Mo 18:15 VMP11 HS

Flex-prints for the Mu3e experiment — •Sebastian Dittmeier

for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg

Mu3e is a novel experiment dedicated to the search for the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a targeted sensitivity of a branching ratio (BR) down to 10^{-16}. Within the standard model of particle physics this process is extremely suppressed to $BR < 10^{-54}$. Thus, any observation would be a clear sign for new physics beyond the standard model. The Mu3e detector consists of a silicon pixel tracking detector using the novel HV-MAPS (High Voltage Monolithic Active Pixel Sensor) technology to measure the momentum of the decay products, and scintillating fibres and tiles for precise timing. The pixel sensors are thinned to $50\mu m$ to achieve a material budget of about 0.1% radiation length per tracking layer. The pixel sensors are powered and connected to readout frontend boards using custom designed flex-prints, which are low material interconnects with a high signal density. We present studies of high speed data transmission up to 3.2 Gb/s over flex-print prototypes produced in-house. The design of the flex-prints for the Mu3e detector will be discussed. A 3-layer design including power, ground and slow control distribution, as well as 9 1.25 Gb/s data transmission lines for the readout of the pixel sensors is foreseen.

T 42.8 Mo 18:30 VMP11 HS

Integration des aktualisierten USBPix Testsystems in die Steuersoftware STcontrol — •Eric Buschmann, Jörn Grosse-Knetter und Arnulf Quadt — Georg-August-Universität Göttingen

Die geplante Luminositätserhöhung des LHC (HL-LHC) vergrößert die Strahlenbelastung der Detektoren und hebt die Ansprüche an Orts- und Zeitauflösung. Dies erfordert eine neue Generation von Sensoren und Auslesechips, welche zu ihrer vollständigen Charakterisierung verbesserte Testsysteme bedingen. USBpix 3 ist die nächste Generation der USB-basierten USBpix Test- und Auslesesysteme, die in Labor- und Teststrahl-Umgebungen verwendet werden. Die neue Hardware ermöglicht hohe Übertragungsraten mit USB 3.0 und bietet Leistungsreserven für zukünftige Entwicklungen. Durch den verwendeten FPGA ist das System flexibel anpassbar. Dabei kommt eine Firmware basierend auf dem modularen Basil-Framework zum Einsatz. Die Steuerung erfolgt über eine graphische Benutzeroberfläche basierend auf der offiziellen ATLAS Pixelsoftware PixLib. Im Vortrag wird das System und dessen Integration in die Steuersoftware STcontrol vorgestellt.