T 118: Trigger und DAQ 3

Zeit: Donnerstag 16:45–18:20 Raum: VSH 05

Gruppenbericht T 118.1 Do 16:45 VSH 05

BonnDAQ - DAQ Software for the Belle II Pixel Detector — Jochen Dingfelder, •Florian Lütticke, Carlos Marinas, and Norbert Wermes for the Belle II-Collaboration — Physikalisches Institut, Rheinische Friedrich-Wilhelms Universität Bonn

The future Belle II experiment at the SuperKEKB accelerator will feature 2 layers of ultra-thin DEPFET pixel detectors, consisting of multiple modules. A DEPFET is a **P**-channel **F**ield **E**ffect **T**ransistor on a fully **DE**pleted bulk. Collected charge drifts into a potential minimum below the transistor gate, thus modulating the drain current. The readout current is digitized and zero suppressed on the module by multiple **A**pplication **S**pecific **I**ntegrated **C**ircuits (ASICs). The data is read out by the DHH (**D**ata **H**andling **H**ybrid), an FPGA based readout system, which processes the data of several modules for further backend electronic during the experiment. For test data taking in lab setups, during beam tests and during local calibration runs in the final experiment, data can be transmitted directly to a computer by the DHH using the **U**ser **D**atagram **P**rotocol (UDP). For receiving, checking and storing data the BonnDAQ software was developed. It features redistribution of data to **D**ata **Q**uality **M**onitoring (DQM) modules, an interface to the Belle II slow control system, lossless online data compression and integration into the EUDAQ Data Acquisition framework. Both C++ and Python modules are available for reading stored files as well as receiving live data. In this talk, the design choices and first performance measurements of the software are discussed and example results from its operation are presented.

T 118.2 Do 17:05 VSH 05

The Data Handling Processor of the Belle II DEPFET Detector — •Leonard Germic, Tomasz Hemperek, Hans Krüger, Carlos Marinas, Jochen Dingfelder, and Norbert Wermes for the Belle II-Collaboration — Universität Bonn

A two layer highly granular DEPFET pixel detector will be operated as the innermost subsystem of the Belle II experiment, at the new Japanese super flavor factory (SuperKEKB). Such a finely segmented system will allow to improve the vertex reconstruction in such ultra high luminosity environment but, at the same time, the raw data stream generated by the 8 million pixel detector will exceed the capability of real-time processing due to its high frame rate, considering the limited material budged and strict space constrains. For this reason a new ASIC, the Data Handling Processor (DHP) is designed to provide data processing at the level of the front-end electronics, such as zero-suppression and common mode correction. Additional feature of the Data Handling Processor is the control block, providing control signals for the on-module ASICs used in the pixel detector. In this contribution, the description of the latest chip revision in TSMC 65 nm technology together with the latest test results of the interface functionality tests are presented.

T 118.3 Do 17:20 VSH 05

DAQ Test System for CMS Tracker Upgrade Phase 2 — Thomas Eichhorn, •Mykyta Haranko, and Andreas Mussgiller — DESY, Hamburg, Germany

For the upcoming high-luminosity phase of the LHC, the tracking detector of the CMS experiment has to be upgraded. Two types of detector modules are foreseen to be used for the outer tracker regions: so-called 2S and PS modules. Each module type consists of two semiconductor sensors with corresponding front-end electronics for the readout.

For the future module production at DESY, testing infrastructure is being developed, based on the FC7 board. The FC7 is a μTCA-compatible Advanced Mezzanine Card for generic data acquisition and control applications. Developed by Imperial College London and built around the Xilinx Kintex 7 FPGA, the FC7 provides a large array of configurable I/O ports, primarily delivered by on-board FPGA Mezzanine Card (FMC) headers, which give the opportunity to establish an optical or electrical interface between the FC7 and the front-end electronics of the CMS tracker's modules.

This talk will present the development status of the FC7 firmware and very first test results.

T 118.4 Do 17:35 VSH 05

Entwicklungen zur Datenauslese des ATLAS Inner Tracker — Gerhard Brandt, •Eric Buschmann, Jörn Grosse-Knetter und Arnulf Quadt — Georg-August-Universität Göttingen

Die erhöhte Luminosität des Large Hadron Colliders (LHC) nach dem geplanten Upgrade zum High Luminosity LHC (HL-LHC) stellt hohe Anforderungen an die Detektor- und Auslesesysteme. Für den ATLAS Detektor am LHC ist hierfür ein vollständiges Ersetzen des jetzigen Inner Detector durch einen vollständig halbleiterbasierten Inner Tracker (ITk) bestehend aus Pixel- und Streifensensoren geplant. Dabei ist eine Strahlenhärte für Fluenzen über 10^{16} neq/cm^2 erforderlich, wofür neue Komponenten wie GBTx und RD53 entwickelt werden. Besonders die Auslese der innersten Pixellagen stellt eine Herausforderung dar und benötigt eine Übertragungsrate von einigen Gb/s pro Modul. Die RCE (Reconfigurable Cluster Element) Plattform integriert ARM Prozessoren mit FPGAs und findet als Test- und Entwicklungsplattform für das ATLAS Upgrade Verwendung. Der aktuelle Stand der Entwicklungen wird vorgestellt.

T 118.5 Do 17:50 VSH 05

Enhanced Bunch Crossing Identification for Saturated Pulses in the ATLAS Level-1 Calorimeter Trigger — •Claire Antel — Kirchhoff-Institut für Physik, Heidelberg

The ATLAS Level-1 Trigger system is designed to perform an ultrafast analysis of a collision provided by the Large Hadron Collider (LHC) in order to to decide within 2.5 microseconds whether to keep the event for further processing. The ATLAS Level-1 *Calorimeter* Trigger participates in this decision by processing calorimeter-based information from the detector. The preprocessing of the signals includes the identification of the correct bunch crossing (BCID) in which the collision took place; failure to do so will lead to events being irrevocably lost.

In view of the increased collision energy in Run II, a new BCID algorithm was commissioned in the Level-1 Calorimeter Trigger that targets saturated pulses. The algorithm is based on new capabilities offered by hardware upgrades in the calorimeter trigger, namely the implementation of new multi-chip modules that have a 80 MHz digitisation rate - twice that of the previous system. The inputs of the algorithm are the 80 MHz digitised samples on the rising edge of the pulse. Thus in order to tune the algorithm, the pulse shapes of signals from physics collision events were studied, using special runs with 80 MHz readout.

The algorithm was commissioned throughout 2016 and enabled towards the end of the year's proton physics data taking period. Presented here is the commissioning as well as the initial performance of the new saturated BCID algorithm.

T 118.6 Do 18:05 VSH 05

FPGA-basierte Spurrekonstruktion für den Ausbau des Experiments CMS (Phase II) — Christian Amstutz, Matthias Balzer, Benjamin Oldenburg, Oliver Sander, •Thomas Schuh und Marc Weber — KIT - Karlsruhe Institute of Technology (DE)

CMS entwickelt für den Hoch-Luminositätsbetrieb ab 2026 einen vollständig neuen auf "pT-Modulen" aufbauenden äußeren Spurdetektor. Dieser wird Treffer von Primärteilchen mit einem Transversalimpuls über 3 GeV/c selektieren und mit der Kollisionsrate des LHC von 40 MHz und einer resultierenden Datenrate von 50 TBit/s auslesen können. Um die Ereignisrate von CMS trotz erhöhter Luminosität zu erhalten, ist es zwingend notwendig bereits in der ersten Ereignisselektion Spurdaten zu verwenden. Dazu müssen die Treffer des äußeren Spurdetektors innerhalb von 4 us zu Spuren rekonstruiert werden. Solch eine auf Teilchenspuren gestützte erste Triggerstufe stellt ein absolutes Novum für ein Hochenergiephysikexperiment dar. Das Systemkonzept, die Architektur, die zugrundeliegenden Algorithmen wie die Hough-Transformation zur Spurfindung werden eingeführt und Ergebnisse eines Demonstrators, welcher ein voll funktionsfähiges und skalierbares Segment des Gesamtsystems darstellt, werden präsentiert.