T 46: Elektronik

Zeit: Dienstag 11:00–12:30 Raum: JUR 5

T 46.1 Di 11:00 JUR 5

KLauS: A low power Silicon Photomultiplier Charge Readout ASIC in 0.18um UMC CMOS Technology — •Konrad Briggl for the CALICE-D-Collaboration — KIP, Universität Heidelberg

The CALICE collaboration is developing highly granular calorimeters fur future linear collider experiments. The high channel count, as well as the little space for cooling infrastructure, pose stringent requirements on the integrated readout electronics, limiting the allowed power consumption to 25uW per channel by the use of powergating techniques. We present the development of KLauS, a low power mixed mode ASIC for charge readout of Silicon Photomultipliers (SiPMs). The analog front-end is designed to achieve sufficient signal to noise ratio for single pixel signals using novel low-gain SiPMs, while allowing charge measurements over the full dynamic range of these sensors. It consists of an input stage, two charge measurement branches and a fast comparator for timestamping and autotriggered operation. A successive approximation register (SAR) ADC with a resolution of 10bits was implemented to digitize the pulse height informations. An additional pipelined SAR stage allows to increase the quantization resolution to 12bit in order to digitize single pixel charge spectra. Characterization measurements and design details of a 7 channel mixed signal prototype ASIC will be presented.

T 46.2 Di 11:15 JUR 5

MuTRiG: a Mixed-Signal SiPM Readout ASIC with High Timing Resolution and High Event Rate Capability — •Huangshan Chen, Konrad Briggl, Patrick Eckert, Tobias Harion, Yonathan Munwes, Wei Shen, Vera Stankova, and Hans-Christian Schultz-Coulon for the Mu3e-Collaboration — Kirchhoff Institut für Physik, Heidelberg University, Heidelberg, Germany

MuTRiG is a mixed-signal Silicon Photomultiplier readout ASIC developed in UMC 180 nm CMOS technology. It is dedicated to the readout of the tile detector and the fiber detector of the Mu3e experiment. A good timing resolution of 100 ps (σ) and 500 ps (σ) is required for the Mu3e tile detector and the Mu3e fiber detector respectively, in order to reduce the accidental background at high rates. An event rate as high as 1.3 MHz/channel in the Mu3e fiber detector poses another challenge for the development of MuTRiG. MuTRiG is designed with 32 fully differential analog front-end channels and 50 ps time binning TDCs, which both have been extensively characterized in STiCv3 ASIC and have proven an excellent timing resolution. The recorded event data are processed by the integrated digital circuits and transferred to the data acquisition system (DAQ) via a gigabit LVDS data link with 8b/10b encoding. The gigabit data link is accomplished by a dedicated double data rate serializer and a customized LVDS transmitter. An external validation functionality is implemented to reduce the load of data link. The design of the MuTRiG chip and the characterization results of the analog front-end, TDC and the gigabit data link will be presented.

T 46.3 Di 11:30 JUR 5

Design of the new testboard for the SPIROC2e BGA package — •Amine Elkhalii for the CALICE-D-Collaboration — Wuppertal University

The CALICE Collaboration is developing calorimeters for a future e^+e^- linear collider. These calorimeters have a high granularity in order to allow Particle Flow Analysis and to achieve a jet energy resolution of 3-4%. One of these concepts is the Analog Hadronic Calorimeter (AHCAL) based on 3×3×0.3 cm^3 scintillator tiles with individual Silicon Photo-multiplier (SiPM) readout. A former physics prototype of the AHCAL has proven the performance and suitably of a such concept. The current focus of the second generation engineering prototype is to have a $1m^3$ detector, which is fully scalable to a linear collider detector with all its constraints. A huge amount of components have therefore to be tested before assembly, including the SPIROC ASIC developed by Omega. This chip provides the readout for 36 SiPMs, including individual bias voltages, self-triggering, timing measurements and 12-bit signal resolution, while maintaining a very low power consumption of 25 μW per channel. Around 1000 of these ASICs have to be characterised and tested for the prototype in 2017. This talk will focus on the development of the test stand and the first results on the testing and characterisation of the chips.

T 46.4 Di 11:45 JUR 5

Design and evaluation of a versatile sub-ns LED pulser — •Martin Rongen and Merlin Schaufel — III. Physikalisches Institut, RWTH Aachen

Many experimental setups for the calibration of photosensors require light sources with sub-nanosecond timing precision. Such sources are commercially available. However, often their costs prohibit applications with large numbers of sources. In contrast, simple circuits commonly used in the community, such as the Kapustinsky pulser, are limited to light pulses of few nanosecond duration. In this talk we present the design and evaluation of a sub-nanosecond light pulser based on an avalanche transistor. The choice of LED paired with variable biasing allows for a wide range of output intensities at an arbitrary wavelength. This device will be used for the timing calibration of photosensors for IceCube-Gen2 and the IceAct air Cherenkov telescope.

T 46.5 Di 12:00 JUR 5

Online Track and Vertex Reconstruction on GPUs for the Mu3e Experiment — •Dorothea vom Bruch for the Mu3e-Collaboration — Institut für Kernphysik, Johannes Gutenberg-Universität Mainz

The Mu3e experiment searches for the lepton flavour violating decay $\mu^+ \to e^+e^-e^+$, aiming at a branching ratio sensitivity better than 10^{-16}. To reach this sensitivity, rates above $10^9 \mu/s$ are required. A high precision silicon tracking detector combined with excellent timing resolution from scintillating fibers and tiles will measure the momenta, vertices and timing of the decay products of muons stopped in the target to suppress background.

During the first phase of the experiment, a rate of $10^8 \mu/s$ will be available, resulting in a data rate of $\sim$ 10 GB/s of zero-suppressed data. The trigger-less readout system consists of optical links and switching FPGAs sending the complete detector data for a time slice to one node of the filter farm. As we can only store $\sim$ 100 MB/s of data, a full online reconstruction is necessary for an event selection. The highly parallel structure of graphics processing units (GPUs) is ideal for this purpose. An FPGA inside the filter farm PC therefore transfers the event data to the GPU via PCIe direct memory access. The GPU finds and fits tracks using a 3D tracking algorithm for multiple scattering dominated resolution. In a second step, a three track vertex selection is performed, reducing the output data rate to below 100 MB/s by removing combinatorial background. The talk discusses the implementation of the track fit and vertex selection on the GPU.

T 46.6 Di 12:15 JUR 5

Flexprint Design Studies for the Mu3e Experiment — •Jens Kröger for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg

The Mu3e experiment will search for the lepton-flavour violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} decays. To reach this sensitivity, an excellent momentum resolution as well as a very good vertex reconstruction are crucial. Since the muons will be stopped before decaying, their decay products will have very low momenta. Hence multiple scattering is a major issue that is tackled by minimizing the material budget of the tracking detector. In order to achieve this, the silicon pixel sensors will be thinned to 50 μm and mounted on flexprints consisting of very thin Kapton and aluminium (and possibly copper) traces for signals, power and ground. The material budget of the flexprints will be less than 0.5 ‰ of the radiation length of aluminium.

This talk will cover the design of the Mu3e pixel detector, focussing on the use of flexprints for the readout and supply of the pixel sensors. Results from measurements with flexprint prototypes as well as future designs will be discussed.