T 94: Pixeldetektoren 4

Zeit: Mittwoch 16:45–19:05 Raum: VSH 116

T 94.1 Mi 16:45 VSH 116

Gated mode operation of large DEPFET pixel modules for the Belle II Pixel Detector — •Felix Müller[1], Christian Kiesling[1], Philipp Philipp[1], Hans-Günther Moser[1], Ladislav Andricek[2], Christian Koffmane[2], Jelena Ninkovic[2], Rainer Richter[2], and Andreas Wassatsch[2] for the Belle II-Collaboration — [1]Max-Planck-Institut für Physik, München — [2]Halbleiterlabor der Max-Planck-Gesellschaft, München

DEPFET pixel detectors offer excellent signal to noise ratio, resolution and low power consumption with very little material budget. They will be used at Belle II and are a candidate for an ILC vertex detector. The modules were fully characterized and the operation voltages and control sequences of the ASICs were investigated and optimized.
Due to the rolling shutter read-out the DEFET modules have integration times in the order of 20 μs, which can create problems in applications with temporary high background at SuperKEKB, e.g. during the top-up injection of bunches which will create large backgrounds every ten microseconds for about a few ms. In order to get rid of this background, we study a new operation mode, which allows a gated or shutter controlled operation of the detector. This operation mode makes the detector blind for short time interval of about 1 microsecond in which background is expected to pass the detector, whereas the charge of the previous signals will not be removed. Simulations and successful lab tests with large DEPFET matrices will be presented.

T 94.2 Mi 17:00 VSH 116

Charge calibration for the read-out chip of the ATLAS Insertable B-Layer — Joern Grosse-Knetter, Arnulf Quadt, and •Paolo Sabatini — II. Physikalisches Institut, Georg-August-Universität Göttingen

The Insertable B-Layer (IBL) is the innermost layer of the ATLAS Pixel detector, composed of 14 staves located around the beam pipe at a distance of about 33 mm, hosting about 12 million hybrid-silicon pixels. A new generation of Front End chips (FE-I4) was developed exclusively for this component, in order to sustain the challenging hit rate and radiation dose. The insertion of this layer improves the performance on secondary vertex recognition (b-tagging) maintaining the total material budget of the detector low.

Being the innermost layer requires a high position resolution, which is improved by algorithms exploiting the measured charge in each pixel of the cluster induced by a crossing particle. This information is obtained, for each pixel, by measuring the Time-over-Threshold (ToT) of the measured signal, expected to be proportional to the deposited charge. That makes the ToT-to-charge calibration important for track position reconstruction and it requires an automatic test and tuning procedure, aimed to ensure the correct charge measurement for each pixel of the detector. This calibration, performed via on-chip charge injection, depends on two conversion factors known to limited precision from wafer probing. New improved calibration ideas based on production and operation data will be presented.

T 94.3 Mi 17:15 VSH 116

Charakterisierung finaler Demonstrationsmodule für den Belle II-Pixelvertexdetektor — Jochen Dingfelder, Leonard Germic, Hans Krüger, •Barbara Leibrock, Florian Lütticke, Carlos Marinas, Botho Paschen und Norbert Wermes für die Belle II-Kollaboration — Universität Bonn, Physikalisches Institut

Im Jahr 2017 wird die Aufrüstung des KEKB-Beschleunigers in Japan fertiggestellt werden. SuperKEKB wird asymmetrische e+e-Kollisionen bei etwa 40-mal höherer Luminosität liefern. Um die höhere Ereignisrate ausnutzen zu können, wird derzeit ein Upgrade des Belle-Detektors zu Belle II durchgeführt. Als wichtiger Teil des Detektor-Upgrades wird ein neuer zweilagiger, auf DEPFET-Technologie basierender Pixeldetektor als innerster Subdetektor hinzugefügt. Die DEPFET-Pixelmatrix besteht aus p-FETs mit einem zusätzlichen internen Gate und vollständig verarmtem Siliziumbulk. Die im Sensor generierten Elektronen driften ins interne Gate und modulieren den Transistorstrom. Die Transistorströme der Pixel werden mit Hilfe des Drain Current Digitizer (DCD) Chips ausgelesen und in digitale Signale umgewandelt. Diese werden im Data Handling Processor (DHP) Chip weiterverarbeitet, in dem eine erste Datenreduktion vorgenommen wird. Um die zuverlässige Zusammenarbeit der unterschiedlichen Komponenten zu gewährleisten, werden sie zunächst mit Demonstrationsmodulen getestet, die ein funktional vollständiges Matrix- und Komponentensystem enthalten. In diesem Vortrag werden Messungen zur systematischen Charakterisierung und Optimierung der aktuellen Version der Demonstrationsmodule vorgestellt.

T 94.4 Mi 17:30 VSH 116

Pixel Readout Chip for ATLAS HL-LHC Hybrid Pixels in 65nm CMOS Technology — Tomasz Hemperek, Tetsuichi Kishishita, Hans Krüger, •Piotr Rymaszewski, Marco Vogt, Tianyang Wang, and Norbert Wermes — University of Bonn, Bonn, Germany

The LHC High Luminosity upgrade will result in a significant change of environment in which particle detectors are going to operate, especially for devices very close to the interaction point like pixel detector electronics. Due to similar requirements in terms of pixel size (50μm $\times$ 50μm), hit rate (3 $\frac{GHz}{cm^2}$), and radiation tolerance (500Mrad) ATLAS and CMS are developing together a pixel readout chip in 65nm CMOS technology to cope with this challenge. This collaboration, named RD53, started in 2013 and is now close to submitting a first large scale prototype. In this talk the chip overview will be presented, which includes the design flow, read-out concept and the development of specialized IP blocks. Issues arising from the very high radiation tolerance requirement will be discussed. A large focus will be given to the parts designed by our group.

T 94.5 Mi 17:45 VSH 116

FE65-P2: A prototype pixel readout chip in 65nm technology for HL-LHC upgrades — Rebecca Carney[2], Markus Cristinziani[1], Mauricio Garcia-Sciveres[2], Dario Gnani[2], •Carlo Alberto Gottardo[1], Timon Heim[2], Tomasz Hemperek[1], Lashkar Kashif[3], Hans Krüger[1], Abderrezak Mekkaoui[2], Veronica Wallagen[2], and Norbert Wermes[1] — [1]Physikalisches Institut, Universität Bonn — [2]Lawrence Berkeley National Lab, Berkeley, CA, USA — [3]University of Wisconsin-Madison, Madison, WI, USA

The High-Lumi LHC upgrade of the trackers of the ATLAS and CMS experiments is a challenging benchmark for silicon detector technology. High rate, radiation hardness, low noise and low power consumption are the main concerns the detector design has to deal with.

The FE65-P2 pixel readout test chip has been developed by the RD53 collaboration with the goal of demonstrating small (50 μm pitch) pixel performance and validating its layout scheme in 65 nm technology. The layout design, dubbed "analog island in a digital sea" is characterized by analog front-end blocks shared by four pixels and surrounded by synthesized digital logic and it nominally operates down to a threshold of 500 electrons.

A description of the readout chip and total ionizing dose (TID) radiation hardness test will be presented.

Several parameters of the chip have been measured during x-ray irradiation up to a dose of 45 Mrad showing both expected and unexpected features.

T 94.6 Mi 18:00 VSH 116

65 nm Pixel Readout-Chip Verification and Characterization Environment for the High-Luminosity Upgrade of the ATLAS Detector within the RD53 Collaboration — Viacheslav Filimonov, Tomasz Hemperek, Fabian Hügging, Jens Janssen, Hans Krüger, David-Leon Pohl, Piotr Rymaszewski, •Marco Vogt, Jochen Dingfelder, and Norbert Wermes — Physikalisches Institut der Universität Bonn

With the LHC High Luminosity upgrade, multiple new challenges will arise for the involved particle detector systems.

Due to significantly increased hit rates, new readout chips with highly complex digital architectures will have to deliver drastically increased data rates and ensure unprecedented radiation tolerance, especially close to the interaction point.

The collaboration "RD53" was formed to approach these challenges, by designing a pixel readout chip in a 65 nm CMOS process, suitable for the inner layers of both the ATLAS and the CMS experiment.

In order to verify the digital design and to characterize the prototype chips, a test and data acquisition environment consisting of software frameworks and custom hardware is currently being developed in Bonn.

One important aspect is the ability to use the same Verilog/Python framework for the hardware as well as during the design verification process.

The concept and status of this test environment will be presented, as well as a summary about the new hybrid pixel readout chip.

T 94.7 Mi 18:15 VSH 116

Characterization of readout circuitry in a demonstrator chip of depleted CMOS active sensors — •Toko Hirono, Tomasz Hemperek, Fabian Hügging, Piotr Rymaszewski, Tianyang Wang, and Norbert Wermes — Physikalisches Institut, Universität Bonn

Depleted CMOS active sensors (DMAPS) in commercial multi-well CMOS technologies are an attractive detector choice for high-energy particle physics experiments, such as in the ATLAS High Luminosity Large Hadron Collider (HL-LHC). Since charge collection by drift is mandatory for such a harsh radiation environment, the application of high bias voltage to high resistive sensor material is needed. A demonstrator of a DMAPS (LFCPIX) has been fabricated in LFoundry 150nm CMOS process on a substrate with a resistivity of >2 kΩ·cm. The chip size is 10 mm × 10 mm and the pixel size is 50 μm × 250 μm. ATLAS HL-LHC requires high time resolution of 25 ns and a total ionizing dose (TID) for the outer layers of ATLAS pixel detector is estimated as high as 50 Mrad. Ten flavors of readout circuitry are implemented in LFCPIX to investigate the timing performances and the radiation hardness. In the presentation, the characteristics of each readout flavors measured with electrical test pulses, radio active sources and 2.5 GeV electron beam will be shown.

Gruppenbericht T 94.8 Mi 18:30 VSH 116

A Thin Silicon Pixel Tracker for the Mu3e Experiment — •Adrian Herkert for the Mu3e-Collaboration — Physikalisches Institut Heidelberg

The Mu3e experiment will search for the charged lepton flavor violating decay $\mu \to eee$, which is suppressed to unobservable levels in the Standard Model. The aim is to either discover it, which would be a clear sign of new pyhsics, or to exclude it above a branching ratio of 10^{-16} at 90% CL. To achieve that, the world's highest intensity muon beam is required, which will be available at the Paul Scherrer Institute (PSI) in Switzerland. The experiment is based on low energy muons being stopped on a target and decaying at rest, which results in decay electrons with energies ≤ 53 MeV. Backgrounds can be suppressed by very precise momentum, vertex and timing measurements. Due to the electrons' low energies, the vertex and momentum resolution are dominated by multiple scattering, which makes a low material budget in the active detector region crucial for the experiment. The other basic requirement is the capability of dealing with muon decay rates of about $10^9 \frac{1}{s}$. A barrel shaped detector system has been designed which consists of four layers of high-voltage monolithic active pixel sensors (HV-MAPS) in a 1T solenoid magnet for tracking and a combination of scintillating fibers and tiles for additional timing measurements.

After a general overview of the Mu3e experiment, this talk will focus on the pixel tracker including the sensors, readout scheme, mechanics and cooling. Performance results of the last sensor prototype, the MuPix7, will be presented.

T 94.9 Mi 18:50 VSH 116

Readout of the Mu3e pixel detector — •Sebastian Dittmeier for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg

The Mu3e experiment searches for the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with a target sensitivity of one in 10^{16} decays. The Mu3e detector consists of an ultra-thin silicon pixel tracking detector using the HV-MAPS (High Voltage Monolithic Active Pixel Sensor) technology to measure the momentum of the decay products, and scintillating fibres and tiles for precise timing.

This talk covers the readout components of the pixel detector. The pixel sensors send their hit information untriggered via fast serial data links to FPGAs located on the frontend boards where the data is time sorted. Via fast optical links, this data is sent to the switching boards where the data from several detector segments is merged into time slices of the full detector and provided to the computing nodes that perform online event reconstruction and filtering based on graphics processing units.

A prototype of the frontend board including the FPGA and optical transceivers has been produced and evaluated. Results of these studies will be presented.