T 5: Pixel-Detektoren I

Zeit: Montag 16:00–18:30 Raum: Philo-HS5

T 5.1 Mo 16:00 Philo-HS5

A Monolithic Pixel Sensor Prototype for the ATLAS Experiment in AMS 180 nm HV-CMOS Technology — •Adrian Herkert[1], Heiko Augustin[1], Niklaus Berger[2], Sebastian Dittmeier[1], Carsten Grzesik[2], Jan Hammerich[1], Lennart Huth[1], David Immig[1], Jens Kröger[1], Ivan Perić[3], Mridula Prathapan[3], André Schöning[1], Iurii Sorokin[2], Alena Weber[3], Dirk Wiedner[1], and Marco Zimmermann[2] — [1]Physikalisches Institut Heidelberg — [2]Institut für Kernphysik Mainz — [3]Karlsruher Institut für Technologie

With the high luminosity upgrade of the LHC accelerator the ATLAS detector will be upgraded too. As part of that the inner tracker (ITK) will be completely exchanged, not only because the current tracker will reach the end of its lifetime at the end of Run 3 but also to cope with the increased pileup. Hybrid pixel and strip detectors are well established technologies and form the baseline of the ITK design as described in two Technical Design Reports. As alternative for the outermost pixel barrel layer, monolithic pixel detectors are considered which combine sensor and readout ASIC in one chip.
ATLASPix1 is, amongst others, a prototype for a monolithic pixel sensor demonstrator. It is produced in the AMS 180 nm HV-CMOS process aH18.
In this talk, the ATLASPix1 sensor will be introduced and first characterization results from several testbeam campaigns will be presented.

T 5.2 Mo 16:15 Philo-HS5

Large area HVCMOS pixel sensor prototype for ATLAS detector upgrade — •Mridula Prathapan, Hui Zhang, Alena Weber, and Ivan Peric — KIT, Karlsruhe, Germany

HVCMOS pixel sensors have been proposed for the upgrade of ATLAS experiment. They are implemented in commercial HVCMOS technologies which makes the production cost effective when compared to hybrid sensors. The HVCMOS detectors are monolithic which means that the readout electronics and the sensor part are implemented on the same substrate. A high voltage is used to create a depletion region where the particle detection occurs. A large area prototype for ATLAS experiment named ATLASpix1 has been designed and fabricated in AMS 180nm high voltage CMOS process technology. ATLASpix1 includes three different design flavours in terms of pixel size and readout logic. The chips have been fabricated using wafers of different resistivity. The sensor contains a pixel matrix and a full readout chain that supports triggering with programmable latency and fast data transmission. A faster readout scheme called Parallel Pixel to Buffer readout (PPtB) has been introduced. Currently we are working on the reticle size (2cm x 2cm) sensor that can be used to construct detector modules for ATLAS experiment. A few design improvements on ATLASpix1 such as electronic circuits for amplitude measurement, time walk correction, hit sorting and readout data formatting have been developed and submitted for fabrication on a test chip. The status of current developments on HVCMOS sensor design in AMS 180nm will be presented with emphasis on design details.

T 5.3 Mo 16:30 Philo-HS5

Charakterisierung von HVCMOS Sensoren für den ATLAS Pixeldetektor — •Felix Ehrler, Ivan Perić und Rudolf Schimassek — IPE, Karlsruher Institut für Technologie

Hochspannungs CMOS (HVCMOS) Pixelsensoren sind verarmte aktive Pixelsensoren, die in einem kommerziellen Standardprozess implementiert sind. Dank ihrer Strahlenhärte und schnellen Signalgeneration werden HVCMOS Sensoren für mehrere Experimente benutzt werden, beziehungsweise sind für diese vorgeschlagen: Mu3e, ATLAS, CLIC.

Im Jahr 2017 wurden vier monolithische HVCMOS Pixelsensoren gemeinsam in der 180 nm Technologie AMS aH18 auf Wafern mit verschiedenen Resistivitäten produziert. Ihre Gesamtfläche beträgt etwa 22×22 mm^2. Ein Sensor zielt auf den Einsatz im Mu3e Experiment ab, während die drei anderen für den Einsatz im ATLAS-Detektor konzipiert sind.

Jeder der vier Sensoren vereint spezielle Eigenschaften in sich, die auf die jeweilige Anwendung zugeschnitten sind. Dazu zählen innovative Konzepte wie die Parallel-Pixel-to-Buffer (PPtB) Auslesearchitektur für höchste Trefferraten, getriggerte Auslese, isolierte PMOS-Transistoren und Timewalk-Korrektur durch Signalhöhenbestimmung.

In diesem Beitrag werden Testergebnisse dieser Sensoren wie allgemeine Funktionalität, Messungen der Orts- und Zeitauflösung bei höchsten Auslesegeschwindigkeiten unter Labor- und Testbeam-Bedingungen präsentiert.

T 5.4 Mo 16:45 Philo-HS5

Characterization of a depleted monolithic active pixel sensor prototype in 130 nm Toshiba technology — •Christian Bespin, Tomasz Hemperek, Toko Hirono, Fabian Hügging, Tetsuichi Kishishita, Hans Krüger, Piotr Rymaszewski, Norbert Wermes, and Jochen Dingfelder — Physikalisches Institut der Universität Bonn

Monolithic active silicon pixel sensors using commercial CMOS technology are currently under investigation for usage in environments with high particle rates and high radiation doses as in the upcoming HL-LHC. A prototype of a depleted monolithic active pixel sensor (DMAPS) in 130 nm Toshiba technology is characterized. It consists of different flavors with a pixel pitch of 20 um and 40 um. The pixels are read out using a 3T circuit. Results from gain and noise measurements are presented together with measurements with radioactive sources and a 2.5 GeV electron beam.

T 5.5 Mo 17:00 Philo-HS5

A 65 nm pixel readout chip in 65 nm process with passive CMOS sensor — •Daniel Coquelin, Michael Daas, Tomek Hemperek, Fabian Hügging, Hans Krüger, David-Leon Pohl, Mark Standke, and Norbert Wermes — Nussallee 12, 53115 Bonn

For the high luminosity LHC the ATLAS detector must be upgraded. The tracking detector will be an all silicon tracker with several layers of hybrid pixel detectors. In view of this upgrade, a pixel readout chip in 65 nm TSMC CMOS process was developed (FE65-p2). It consists of 64x64 pixels with a pitch of 50 x 50 um. A passive CMOS sensor from Lfoundry in 130 nm CMOS process with small 50 x 50 um pixels and a bulk resistivity of 4-5 kOhm-cm is bump bonded to the readout chip. The prototype sensor is characterized using IV curves, threshold measurements, as well as electron and X-ray sources.

T 5.6 Mo 17:15 Philo-HS5

Planare n$^+$-in-n Quadmodule für das ITk-Upgrade des ATLAS-Experiments — Silke Altenheiner[1], Sascha Dungs[1,2], •Andreas Gisen[1], Claus Gössling[1], Valerie Hohm[1], Reiner Klingenberg[1], Kevin Kröninger[1], Anna-Katharina Raytarowski[1] und Mareike Weers[1] — [1]TU Dortmund, Experimentelle Physik IV — [2]CERN

Um den Anforderungen des High Luminosity LHC (HL-LHC) gerecht werden zu können, wird es nötig sein, den aktuellen Tracker des ATLAS-Experiments zu ersetzen. Deswegen wird derzeit ein neuer Spurdetektor geplant, der sogenannte Inner Tracker (ITk). In dessen Pixeldetektor sind auch Vierchip- bzw. Quadmodule vorgesehen. Diese bestehen aus einem Siliziumsensor, der zusammen mit vier Auslesechips eine Einheit bildet.

Der derzeitige innerste Spurdetektor des ATLAS-Experiments besteht aus planaren n$^+$-in-n-Silizium-Pixelsensoren. Aus vergleichbaren Sensoren und vier FE-I4 Auslesechips wurden erste Prototypen planarer n$^+$-in-n Quadmodule hergestellt. Diese wurden im Labor und im Testbeam charakterisiert. Dabei wurde der Schwerpunkt auf die Regionen zwischen den Auslesechips gelegt, besonders auf den zentralen Bereich zwischen den vier Auslesechips. Dort auf dem Sensor befinden sich spezielle Pixelzellen, die die Lücke zwischen den Auslesechips berücksichtigen. Ein Quadmodul wurde am CERN-PS mit Protonen bestrahlt und danach erneut im Testbeam charakterisiert.

Dieser Beitrag stellt die Ergebnisse dieser Messungen vor.

T 5.7 Mo 17:30 Philo-HS5

TCAD Simulation for the study of the MuPix Sensor — •Annie Meneses Gonzalez for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg, Germany

The goal of the Mu3e experiment is to search for the lepton flavor violation decay $\mu^+ \to e^+e^-e^+$ with an ultimate sensitivity (in phase II) of one in 10^{16} μ -decays, four orders of magnitude better than the current experimental limit. This gain is considered possible by fully

exploiting advances in silicon detector technologies, data transfer, and processing.

The main challenges of the experiment are to run in a high rate muon beam, excellent momentum resolution and precise vertex and timing resolution. Due to the low momenta of the decays electrons, multiple Coulomb scattering is dominating the momentum measurement precision. The Mu3e pixel tracker is based on thin High-Voltage Monolithic Active Pixel Sensors which allows to integrate sensor and readout functionalities in the same device, reducing the material budget and improving the momentum resolution.

Technology Computer Aided Design (TCAD) is used to develop and optimize semiconductor processing technologies and devices. In this work results from TCAD Simulation on the charge collection time of the MuPix7 sensor are presented and compared to experimental data for different bias voltages and hits positions inside the pixel cell. Using the same physics model, some main characteristics of the MuPix8 prototype are also presented.

T 5.8 Mo 17:45 Philo-HS5

The First Large Scale Fully Monolithic HV-CMOS Sensor: MuPix8 — •Heiko Augustin[1], Alena Larissa Weber[1,2], Mridula Prathapan[2], and Ivan Peric[2] for the Mu3e-Collaboration — [1]Physikalisches Institut Heidelberg — [2]Karlsruher Institut für Technologie

The Mu3e experiment is dedicated to the search for the lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ with an unprecedented sensitivity of one in 10^{16} decays. In the Standard Model this decay is suppressed to a branching ratio below 10^{-54}. Thus, any observation of a signal is a clear sign for New Physics. To reach the sensitivity goal a pixel tracker with low material budget and high rate capability is required. The technology of choice are High Voltage Monolithic Active Pixel Sensors (HV-MAPS) produced in the AMS aH18 180 nm HV-CMOS process, which allows to build fast pixel detectors thinned to 50 μm.

In this talk the architecture of the first large $2 \times 1\,\mathrm{cm}^2$ prototype MuPix8 is presented. It houses three 1.25 Gbit/s data links and tests circuits for timewalk suppression, aiming at a time resolution below 10 ns.

Further the next step towards a full module integration of the final pixel sensor with the test of a reduced slow control scheme on the MuPix9 chip is presented.

T 5.9 Mo 18:00 Philo-HS5

First results from the MuPix8, a large HV-MAPS prototype — •Jan Hammerich for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg

The Mu3e experiment is searching for the charged lepton flavor violating (cLFV) decay $\mu \to eee$ with a planned sensitivity of 1 in 10^{15} decays for phase 1. To achieve such a sensitivity, a fast, high resolution tracking detector is required which has a material budget of 1 ‰ to reduce multiple Coulomb scattering.

A suitable technology for these requirements is the High Voltage Monolithic Active Pixel Sensor (HV-MAPS) concept. It combines fast charge collection via drift with a fully monolithic architecture of sensor and readout in one chip which can be thinned to 50 μm.

The MuPix8 is the first large scale HV-MAPS prototype for Mu3e with a size of $1 \times 2\,cm^2$. Efficiency and time resolution have been measured in testbeam campaigns at DESY. Additionally, measurements with testpulses and radioactive sources are presented.

T 5.10 Mo 18:15 Philo-HS5

MuPix9 - a HV-MAPS prototype with serial powering — •Alena Larissa Weber[1,2], Heiko Augustin[1], Mridula Prathapan[2], and Ivan Peric[2] — [1]Physikalisches Institut Heidelberg — [2]Karlsruher Institut für Technologie

The Mu3e experiment is searching for the charged lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} decays (in phase II). The core elements of the detector are High Voltage Monolithic Active Pixel Sensors (HV-MAPS) which are designed and produced in the AMS aH18 HV-CMOS process with a minimal gate length of 180nm.

In 2017 a large prototype (1 x 2 cm^2) called MuPix8 was submitted, produced and passed the first tests successfully. Currently, we are working towards the final MuPix design. For the final version several new features are required regarding the powering and the command decoder. To test new circuits, a smaller sensor prototype was developed, the MuPix9. On this chip, novel serial powering concepts for the Mu3e experiment were realized using two power regulators. Furthermore the powering of the analog and digital part was separated. Serial powering concepts enable significant reduction of the power supply current and necessary power connections to the sensor-chip.

In this talk different concepts of serial powering for the MuPix sensor and the architecture of the MuPix9 will be presented.