T 27: Halbleiterdetektoren II

Zeit: Dienstag 16:00–18:30 Raum: H03

T 27.1 Di 16:00 H03

On the path to module integration with the HV-MAPS prototype MuPix9 — •Heiko Augustin[1], Alena Larissa Weber[1,2], and Ivan Perić[2] for the Mu3e-Collaboration — [1]Physikalisches Institut Heidelberg — [2]Karlsruher Institut für Technologie

The Mu3e experiment is dedicated to the search for the charged lepton flavour violating decay $\mu^+ \rightarrow e^+e^-e^+$ with an unprecedented sensitivity of one in 10^{16} decays. In the Standard Model this decay is suppressed to a branching ratio below 10^{-54}. Thus, any observation of a signal is a clear sign for New Physics. To reach the sensitivity goal a pixel tracker with low material budget and high rate capability is required. The technology of choice are High Voltage Monolithic Active Pixel Sensors (HV-MAPS) produced in the AMS aH18 180 nm HV-CMOS process, which allows to build fast pixel detectors thinned to 50 μm.

In this talk the architecture and test structures of the MuPix9 prototype are presented. It houses a shunt regulator and a fully monolithic pixel sensor engineered for the use within a serial powering chain. Further it contains a synthesized slow control statemachine aiming to reduce the slow control complexity in the view of module integration.

First results on the MuPix9 performance are presented and the road map for the module integration is depicted.

T 27.2 Di 16:15 H03

The MuPix10 - the current state of design — •Alena Weber for the Mu3e-Collaboration — Physikalisches Institut Heidelberg — Karlsruher Institut für Technologie

The Mu3e experiment is searching for the charged lepton flavor violating decay $\mu^+ \rightarrow e^+e^-e^+$ with a sensitivity of one in 10^{16} decays (in phase II). High Voltage Monolithic Active Pixel Sensors (HV-MAPS) will be used in four tracking layers.

In the last years, several prototypes of different size have been designed and tested. In 2017, a first large prototype (MuPix8) with a size of 1 x 2 cm^2 was submitted and successfully tested. Another small prototype, the MuPix9, has been developed to test several small circuits. The next important design step is MuPix10, which has a full recticle size (about 2 x 2 cm^2). The design should fulfill all Mu3e requirements and be close to the final version to be installed in the experiment. Several design blocks undergo a redesign for a better energy and time resolution and for a more uniform voltage supply inside the chip. Furthermore, the design has to be ported to a new fabrication process (TSI 180 nm HVCMOS).

In this talk, the current state of the MuPix10 design will be presented.

T 27.3 Di 16:30 H03

Qualification of a pixel sensor prototype produced by TSI — •Christoph Blattgerste for the Mu3e-Collaboration — Physikalisches Institut, Universität Heidelberg

High Voltage Monolithic Active Pixel Sensors (HV-MAPS) are suitable for particle physics experiments because they allow for high rate capability at low material budget and costs. HV-MAPS are fully integrated, can therefore be thinned to 50 μm and thus multiple Coulomb scattering is reduced. The strong electric field in the depletion zone allows for fast charge collection via drift and a good time resolution.

The MuPix7, the first fully integrated HV-MAPS prototype, has been produced in the commercial 180 nm HV-CMOS process by the foundries AMS and TSI.

The relevant parameters of the two sensors are compared.

T 27.4 Di 16:45 H03

Measurement Results on Monolithic LFoundry HVCMOS Sensors — •Rudolf Schimassek and Ivan Perić — Karlsruher Institut für Technologie (KIT), Karlsruhe, Deutschland

HVCMOS pixel sensors are depleted active pixel sensors produced in commercial standard CMOS processes. Fast signal generation as well as radiation hardness make them an option for particle physics. Monolithic HVCMOS sensors also have a low material budget.

Typically, time resolution is limited by the power consumption of the pixel amplifiers. To overcome this limitation, signal to noise ratio has to be increased or innovative compensation means have to be implemented.

In LFoundry LF15A (150nm) HVCMOS process, two sensors were produced for process evaluation and development of features for future detectors. One evaluation feature is pixel trimming equalising the pixel characteristics enabling lower thresholds. Features for future detectors are parallel pixel to buffer (PPtB) readout for high rate environments and in-pixel sampling of the signal for improved time resolution.

In this contribution, test results of the detector chips will be presented.

T 27.5 Di 17:00 H03

Characterisation of a depleted monolithic active pixel sensor in 180 nm TowerJazz CMOS technology — Ivan Berdalovic[2], •Christian Bespin[1], Ivan Caicedo[1], Tomasz Hemperek[1], Toko Hirono[1], Fabian Hügging[1], Hans Krüger[1], Thanusan Kugathasan[2], Cesar Augusto Marin Tobon[2], Konstantinos Moustakas[1], Heinz Pernegger[2], Piotr Rymaszewski[1], Walter Snoeys[2], Tianyang Wang[1], Norbert Wermes[1], and Jochen Dingfelder[1] — [1]Physikalisches Institut, Universität Bonn, Bonn, Deutschland — [2]CERN, Genf, Schweiz

Monolithic active silicon pixel sensors using commercial CMOS processes are currently under investigation for the upgrade of the ATLAS pixel detector at the upcoming HL-LHC. The TJ-MonoPix chip is a depleted monolithic active pixel sensor fabricated in 180 nm TowerJazz technology using a small fill factor design. The pixel pitch is 36 μm x 40 μm and the hit information is read out using a FE-I3-like column drain architecture.

Results are presented for unirradiated and irradiated sensors from measurements with radioactive sources and testbeams with 2.5 GeV electrons.

T 27.6 Di 17:15 H03

Active pixel sensor with small pixel size designed for capacitive readout with RD53 ASIC — •Hui Zhang and Ivan Peric — Karlsruher Institut für Technologie

We are designing HVCMOS sensors for several particle physics experiments. These sensors are simple and low cost alternative to classical hybrid detectors. HVCMOS sensor can either contain readout circuits on chip (monolithic sensors) or they can be readout by an external readout ASIC by means of capacitive signal transmission (capacitively coupled hybrid particle detector - CCPD). Both approaches have certain advantages. The detector chip for a CCPD has been implemented in an 180nm HVCMOS process. Depleted high voltage n-well/p-substrate diodes are used as sensors. Every pixel has a size of 25μm x 50μm and contains a charge sensitive amplifier and a simple comparator. The outputs of two pixel comparators are connected to a transmitting electrode (pitch 50μm x 50μm) implemented in the top metal layer of the sensor chip. A process modification has been done specially for this chip - deep p allows implementation of comparators in pixel. The readout chip and the sensor chip can be mechanically connected either by glue (standard option) or as a novel approach with a small number of large bump bonds. The output signals of the sensor chip are transmitted capacitively to the input pads of the readout chip which are connected to the signal receivers. Parameters such as amplitude, pulse width, rise time and signal noise ratio have been measured. In this talk, the sensor design and the measurement results will be presented.

T 27.7 Di 17:30 H03

Design of HVCMOS pixel sensor chips for ATLAS ITk upgrade — •Mridula Prathapan — Karlsruhe Institute of Technology, Karlsruhe, Germany

The high voltage CMOS (HVCMOS) pixel sensors are designed to meet the specifications for the outer pixel layers ATLAS ITk. The HVCMOS prototypes are large fill factor designs in 180nm process on high resistivity substrates. The readout architecture is crucial for achieving high detection efficiencies for high particle hit rates such as 2 MHz/mm^2 in the outer layers of the ITk pixel tracker. The first generation (0.33 cm × 1.3 cm) HVCMOS prototype ATLASpix1_M2 featured a triggered readout scheme with parallel hit transfer from pixels to hit buffers (pptB) and Content Addressable Buffer readout (CAB). Various laboratory tests and irradiation studies have been conducted on ATLASpix1_M2 and is proven to be working. ATLASpix2 is a (3.7

mm × 4.2 mm) MPW run which is optimized for better time resolution and faster readout than its predecessor ATLASpix1_M2. Three novel design concepts namely, programmable sorted readout, hit neighbour logic and smart pixel grouping are introduced in ATLASpix2. Several design improvements are made for ATLASpix3, which is 2×2 cm^2. ATLASpix3 will be used for construction of the HVCMOS demonstrator quad module. This work presents the design evolution of ATLASpix chips in detail together with some measurement results.

T 27.8 Di 17:45 H03

Performance and outlook of a large fill-factor DMAPS in a 150nm CMOS process for the ATLAS HL-LHC upgrade — •Ivan Caicedo, Christian Bespin, Jochen Dingfelder, Tomasz Hemperek, Toko Hirono, Fabian Hügging, Hans Krüger, Piotr Rymaszewski, Tianyang Wang, and Norbert Wermes — Physikalisches Institut, Universität Bonn. Bonn, Germany.

Monolithic CMOS active pixel sensors in depleted substrates (DMAPS) are under consideration for the upgrade of the outer pixel layers of the ATLAS experiment at the LHC. In this upgrade, the area of the pixel modules will be increased tenfold and the so-called HL-LHC is expected to reach a luminosity of $7.5x10^{34}cm^{-2}s^{-1}$. The high collision rate will result in NIEL and TID radiation damage levels of $10^{15}n_{eq}/cm^2$ and 80 Mrad in the outermost pixel region of the inner tracker by the end of operation. Manufacturing DMAPS in a CMOS process reduces the costs and time for large volume production. Thanks to technology add-ons and careful design the sensor collects charge through drift, which improves its efficiency after irradiation.

This talk will summarize the performance of LF-MONOPIX01: a large fill-factor DMAPS designed in a 150nm CMOS process on a highly resistive substrate. The chip was successfully read out by a fast synchronous architecture and back-side processed after thinning down to 200μm. It showed a small noise increase and hit detection efficiency of $\sim$ 99% after irradiation up to the dose levels expected in the HL-LHC. At the end of the presentation, the plans for future design efforts based on the encouraging results will be introduced.

T 27.9 Di 18:00 H03

Lab characterization of the ATLASPix1 — •David Maximilian Immig for the ATLAS AMS/TSI-CMOS-Pixel-Collaboration — Physikalisches Institut, Universität Heidelberg

For the operation at the High Luminosity Large Hadron Collider (HL-LHC) the ATLAS Inner Tracker (ITk) will by fully replaced. The increase of the instantaneous luminosity to 5-7 times the nominal value of LHC sets new challenges for the pixel modules regarding radiation tolerance and readout capability. For the outermost pixel layer alternatives to the hybrid detector baseline technology are considered. Their feasibility with respect to the previous mentioned requirements has to be proven. A promising prototype is the ATLASPix1, a High Voltage Monolithic Active Pixel Sensor (HV-MAPS) produced in the aH18 process by AMS. This technology combines fast charge collection via drift of an active pixel matrix with a full readout in a monolithic architecture.
This talk covers the latest results from lab measurements for the characterization of ATLASPix1.

T 27.10 Di 18:15 H03

Annealing and Characterization of Irradiated Low Gain Avalanche Detectors — •Moritz Wiehe[1,2], Marcos Fernández García[1,3], Michael Moll[1], Sofia Otero Ugobono[1,4], Ulrich Parzefall[2], and Ana Ventura Barroso[5] — [1]CERN — [2]Albert-Ludwigs Universität Freiburg — [3]Universidad de Cantabria — [4]Universidad de Santiago de Compostela — [5]Universitat de Barcelona

Irradiated Low Gain Avalanche Detectors (LGADs) are investigated using the Transient Current Technique (TCT) and IV/CV measurements. The sensors are irradiated to a fluence of 1e14 neq/cm2. For different annealing times (at 60°C), the collected charge, the gain and the electric field profile is measured.