T 91: Elektronik

Zeit: Donnerstag 16:00–18:30 Raum: S02

T 91.1 Do 16:00 S02

ALTAS New Small Wheel Project - Front-End Board Cooling — •Vladisalvs Plesanovs, Ulrich Landgraf, and Stephanie Zimmermann — Universität Freiburg, Freiburg im Breisgau, Germany

For the New Small Wheel (NSW) project the innermost end-cap of the ATLAS muon spectrometer will be replaced. This part of the muon tracking system will use the sTGC and Micromegas detector technologies. The high density of the readout channels of both detector installations results in a high density of the Front-End readout boards (FEBs). To extend the service time of the FEBs their cooling is necessary.

To achieve this goal, an approach that enables FEB cooling with a combination of custom design aluminium plates and heat conducting gap pad was developed and studied. Furthermore, a method for the heat transfer from the transceivers, which are located on the FEB side opposite to the cooling installations, was developed. Four types of measurements were executed to test applicability of both cooling solutions under the NSW cooling system constraints.

The presentation focuses on the cooling test results of the MMFE-8 production board and L1DDC transceivers. The constraints of each task are described and test results of the implemented solution are discussed.

T 91.2 Do 16:15 S02

Effects of humidity on deformation of PCBs in the ATLAS New Small Wheel — •Yanwen Hong, Ulrich Landgraf, and Stephanie Zimmermann — Universität Freiburg

The New Small Wheel (NSW) will replace the present Small Wheel for the Muon Spectrometer upgrade of the ATLAS experiment during the Long Shutdown 2 in next years. Small-strips Thin Gap Chamber (sTGC) and Micro-Mesh- Gaseous Detectors (Micromegas) technologies will be employed in the NSW. Printed circuit boards (PCBs) are widely used in Micromegas readout boards and the sTGC. Unfortunately the humid environment can cause deformation of the PCBs during the transportation, storage process and assembly of the NSW. This deformation misplaces the readout strip pattern and furthermore has a direct impact on the spatial resolution of the detectors. In this context, a closed chamber which can be flushed with controlled humidity density nitrogen was designed and built and a high precision Coordinate Measurement Machine is used to measure the deformation of the sTGC board and Micromegas panel over the large dimensions up to 2 m. Later on, a 3D reconstruction will be achieved to study the deformation in both Z direction and XY-plane. In this talk, the setup of the measurement system is discussed and first measurement results are presented.

T 91.3 Do 16:30 S02

Optimization of the ATLAS (s)MDT readout electronics for high counting rates — Oliver Kortner, Hubert Kroha, and •Korbinian Schmidt-Sommerfeld — Max-Planck-Institut für Physik (Werner-Heisenberg-Institut), Föhringer Ring 6, 80805 München

In the ATLAS muon spectrometer, Monitored Drift Tube (MDT) chambers are used for precise muon track measurement. For the high background rates expected at HL-LHC, which are mainly due to neutrons and photons produced by interactions of the proton collision products in the detector and shielding, new small-diameter Muon Drift Tube (sMDT)-chambers with half the drift tube diameter of the MDT-chambers and ten times higher rate capability have been developed. In order to avoid baseline shifts of the shaped signal the standard MDT readout electronics uses bipolar shaping which, however, leads to a deterioration of signal pulses due to preceding background hits at high counting rates, leading to losses in muon efficiency and drift tube spatial resolution. These so-called signal pile-up effects can be mitigated by active baseline restoration (BLR), which can also eliminate the baseline shift in the case of unipolar shaping. Discrete multi-channel prototype electronics of both types have been tested with generated input pulses and in the Gamma Irradiation Facility at CERN under high γ-irradiation rates.

T 91.4 Do 16:45 S02

CMS DT system electronics upgrade and verification — •Dmitry Eliseev, Thomas Hebbeker, Kerstin Hoepfner, Carsten Heidemann, Giovanni Mocellin, Henning Keller, and Archie Sharma — III. Physikalisches Institut A. RWTH Aachen University, Aachen

The Drift Tube (DT) system is the key detector in the region of the CMS barrel dedicated to the measurement of muon tracks. The signals from a huge number of the DT chambers must be acquired fast and synchronously in order to deliver the information about the hits. In the context of increasing the luminosity of the LHC in preparation for the Phase II the DT system is being upgraded. The main focus of this upgrade is the development of a new generation of read out electronics based on the FPGA technology. The new electronics will provide for the DT system higher acquisition rates, radiation resistance and flexibility of the trigger settings. The development of the new generation instrumentation requires numerous verification measurements. For these purposes a cosmic muon test stand is currently being redesigned and improved at RWTH Aachen. This test stand combines different types of detector technologies providing redundancy and therefore turning it to an excellent verification facility for the new generation electronics of the DT system. This talk presents the status of the DT system upgrade with the main focus on the upgrade of the read out electronics and gives the overview of the Aachen cosmic muon test stand.

T 91.5 Do 17:00 S02

Development of a CANopen node used as a DCS Controller in the ATLAS pixel detector — •Rizwan Ahmad[1], Tobias Fröse[2], Michael Karagounis[2], Susanne Kersten[1], Niklaus Lehmann[1], and Christian Zeitnitz[1] — [1]University of Wuppertal, Wuppertal, Germany — [2]University of Applied Sciences and Arts, Dortmund, Germany

A phase-II upgrade is planned for the ATLAS pixel detector. In this context, the ATLAS pixel detector will get a new DCS (Detector Control System) which is being developed at the University of Wuppertal. The DCS system has three main entities. The DCS Computer (Main Control room), the DCS controller chip and the PSPP (Pixel Serial Powering Protection) Chip. The DCS controller communicates to the DCS computer over CAN (Controller Area Network) bus while the DCS controller communicates to the PSPP chip over SCB (Serial Control Bus), a modified version of the I2C. The DCS controller provides a bridge logic which translates messages between two different communication protocols. It will also implement the CANopen standard in hardwired logic. Additionally, it allows for connecting NTCs to monitor temperature. The DCS controller must be radiation hard up to an ionizing dose of $>$ 500Mrad and it must also provide great immunity against SEU (Single Event Upsets). The first prototype of the chip implements the physical layers for the CAN & SCB and the on-chip voltage regulators. In this talk, the results from the first prototype and the logic implemented on an FPGA will be presented.

T 91.6 Do 17:15 S02

Finaler Prototyp für den Kontroll-Chip des ATLAS Pixel Detektor — •Niklaus Lehmann[1], Rizwan Ahmad[1], Michael Karagounis[2], Susanne Kersten[1] und Christian Zeitnitz[1] — [1]Bergische Universität Wuppertal — [2]Fachhochschule Dortmund

An der Bergischen Universität Wuppertal wird das Detektor-Kontroll-System (DCS) für das Phase II Upgrade des ATLAS Pixeldetektors entwickelt. Dieses beinhaltet zwei ASICs welche die zu überwachenden Messwerte digitalisieren und zum zentralen DCS übertragen. Der Pixel Serial Power Protection (PSPP) Chip ist in der vierten Version vorhanden und ist ein Prototype von einem der beiden ASICs. Der PSPP kann ein einzelnes Modul in einer seriellen Versorgungskette überwachen und bei Bedarf ausschalten. Der Chip wurde entwickelt um parallel zu den Pixel Modulen zu arbeiten. Er kann bis zu 8A an Strom schalten und wird über AC gekoppelte Kommunikationsleitungen angesprochen. Der ganze Chip muss strahlenhart bis zu einer ionisierender Dosis (TID) $>$500Mrad sein und soll robust gegen strahlungsbedingte Bitfehler (SEU) sein. Basierend auf diesem Prototypen, soll dann ein Produktionschip entwickelt werden, welcher im ATLAS Detektor eingebaut werden kann. Resultate der Belastungstests und Bestrahlungen des PSPPs bezüglich SEU und TID werden in diesem Vortrag präsentiert.

T 91.7 Do 17:30 S02

A silicon-photomultiplier readout integrated circuit for highly granular imaging calorimetry — •Zhenxiong Yuan — Kirchhoff Institute for Physics, 69120 Heidelberg, Germany

The KLauS ASIC is a 36-channel mixed-mode silicon-photomultiplier (SiPM) charge readout integrated circuit dedicated to the application in a highly granular imaging calorimeter at a future linear collider experiment. The high density of readout channels together with the dense structure of the calorimeter system limit the readout electronics power consumption down to 25 μW per channel. This ASIC is designed to read out the SiPM signals with high precision and over a large dynamic range with high linearity. Each channel consists of an analog front-end for charge integration and a 10/12-bit ADC to digitize the pulse height information. The design of the ASIC and results of the characterization measurements will be presented. In addition, the integration of the ASIC into the AHCAL calorimeter prototype of the CALICE collaboration is ongoing and the status will also be reported.

Furthermore, a 200 ps bin-sized TDC has been designed for the next version of the KLauS chip, which is implemented to digitize the timing information for the arriving signals. This will allow to study the time development of hadronic showers in the calorimeter with subnanosecond resolution.

T 91.8 Do 17:45 S02

Remote Configuration of the iPMT ReadOutBoard in OSIRIS — Feng Gao, Florian Kiel, Tim Kuhlbusch, Achim Stahl, •Jochen Steinmann, Christopher Wiebusch, and Christian Wysotzki — III. Physikalisches Institut B, RWTH Aachen University

Within a novel concept for photomultiplier readout, all necessary electronics are mounted at the back of the PMT. This introduces the problem, that there is no direct access to the electronics anymore. Configuration and debugging using standard tools and adapters is not possible.

In order to be able to configure and debug the readout-electronics the Slow Control and Configuration Unit has been developed. This device enables programming and configuration of the used FPGA and ADC. Furthermore it provides access to various interfaces, which can be used to implement the slow control and monitoring of the electronics. The whole data transfer is done via Ethernet. Hence no attention has to be payed to the distances between the control system and the PMT.

T 91.9 Do 18:00 S02

Design of a Flexible PCB prototype for the High Granularity Timing Detector at ATLAS — •Maria Soledad Robles Manzano[1,2], Peter Bernhard[2], Andrea Brogna[2], Atila Kurt[2], Lucia Masetti[1,2], Paul Plattner[1], and Quirin Weitzel[2] — [1]Institut für Physik, Johannes-Gütenberg Universität Mainz — [2]Exzellenzcluster PRISMA, Johannes-Gütenberg Universität Mainz

The High-Granularity Timing Detector (HGTD) is designed to improve the physics performance in the forward region of the ATLAS detector when the new HL-LHC is operative. Based on Low Gain Avalanch Detectors, the HGTD will mitigate the pile-up in the forward region by providing a timing resolution below 30 ps per track. In this scenario, the HGTD requirements for data transmission (1.28 Gb/s), sensor powering (up to 1 kV) as well as the geometrical constraints (thickness below 350 μm) lead to the need of custom designed electronics. A Flexible PCB (FLEX cable) is the best candidate to fulfil both the electrical and geometrical requirements. The design of the first prototype is presented.

T 91.10 Do 18:15 S02

Tests of a first prototype of the Flexible PCB for the High Granularity Timing Detector at ATLAS — •Paul Plattner[1], Peter Bernhard[2], Andrea Brogna[2], Atila Kurt[2], Lucia Masetti[1,2], Maria Soledad Robles Manzano[1,2], and Quirin Weitzel[2] — [1]Institut für Physik, Johannes-Gütenberg Universität Mainz — [2]Exzellenzcluster PRISMA, Johannes-Gütenberg Universität Mainz

The High Granularity Timing Detector (HGTD) is proposed for the ATLAS Phase II Upgrade to provide precise timing to tracks in the forward region. Each of its modules will be connected to the peripheral electronics via a flexible PCB. A first prototype of this Flexible PCB has been designed and manufacured. The geometrical constraints (thickness < 350 μm and a maximum length of 750 mm) as well as the electrical requirements (high-speed rate of 1.28 Gb/s and sensor powering up to 1 kV) requires a specific testing plan to check its performance. The Power Integrity (PI) simulation provides the resitance of the dedicated planes for powering and grouding before manufacturing and simulated results are compared to the measured values in the laboratory. The High Voltage insulation of the materials used to fabricate the FLEX cable is also tested. Time Domain Reflectrometry measurements, in order to check the impedance homogeneity of the tracks crucial for Signal Integrity (SI), are performed. Results of the testing of the prototype are presented.