HK 8: Instrumentation II

Zeit: Montag 14:00–16:00 Raum: HS 12

HK 8.1 Mo 14:00 HS 12

New trigger concepts for future measurements at the M2 beam line at CERN — •Benjamin Moritz Veit — CERN and Institut für Kernphysik der Johannes Gutenberg-Universität, Mainz, Deutschland

Currently proposals are being prepared for future measurements with muon and hadron beams at the M2 beam line of the CERN SPS. It is mandatory for these experiments to have a new digital trigger system, which can handle the high rates at the M2 beam line and is flexible in design to adapt for the different planed physics programs. One of the planed experiments is the measurement of the proton radius by elastic muon proton scattering. For this measurement the trigger system has to be sensitive to very small scattering angles for low Q^2 events resulting in very high rates. The new trigger system has to be integrated in the main DAQ and is based on an continuous readout of fast detectors like hodoscopes and scintillating fibre stations. The handling of the triggerless data stream is done by a network of FPGAs performing the multi level trigger decision.

This talk will summarize the plans and the current status of the development of such a trigger-system.

HK 8.2 Mo 14:15 HS 12

Calibration of the Energy-Sum Trigger for the Crystal Barrel Calorimeter at ELSA — •Sebastian Ciupka, Christian Honisch, Michael Lang, Johannes Müllers, Martin Urban, and Reinhard Beck for the CBELSA/TAPS-Collaboration — Helmholtz-Institut für Strahlen- und Kernphysik, Bonn

The Crystal Barrel Calorimeter at the electron accelerator ELSA in Bonn, is used to detect photons from meson decays. The number of clusters produced by the photons is used in the trigger. This talk presents an upcoming upgrade which will include a fast analogous energy-sum in the trigger, allowing the suppression of specific signatures. The summation over 1320 CsI(Tl) detectors is realised in two steps, in a first step the signal of one sector, consisting of up to 23 channels, will be summed up, resulting in 60 individual signals, which will be added together in a second step.

Crucial for setting a precise energy threshold is the calibration of the individual channels of the electronics, performing the summation. This talk will present the current status of the prototype development for the first summation step, show its performance and discuss different calibration methods, as well as the achieved precision.

HK 8.3 Mo 14:30 HS 12

Functionality tests of the SerialAdapter ASIC for the PANDA Calorimeter front-end bus system* — •Christopher Hahn for the PANDA-Collaboration — II. Physikalisches Institut, Justus Liebig Universität, Gießen, Deutschland

The control of the high voltage adjustment for the Large Avalanche Photodiodes of the Electromagnetic Calorimeter (EMC) for the upcoming PANDA experiment at the future FAIR complex in Darmstadt demands innovative and specialised electronics in order to meet the design goals with respect to resolution, timing and spacial constraints. Dedicated hardware chips, the so called SerialAdapter ASICs, were developed at the Gesellschaft für Schwerionenforschung in Darmstadt (GSI Darmstadt). They unite different bus systems and therefore reduce the amount of slow-control cables within the detector volume. These chips are also utilized for the communication and control of the APFEL preamplifier ASICs, which read out the APD photodetectors. To confirm that the different features of the SerialAdapter ASIC work as expected, tests were undertaken. The results of these functionality tests of the ASIC will be presented in this talk.

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HK 8.4 Mo 14:45 HS 12

High-density interconnection technologies for the CBM Silicon Tracking System — •Patrick Pfistner[1], Thomas Blank[1], Michele Caselle[1], Marc Weber[1], Johann Heuser[2], Christian J. Schmidt[2], Carmen Simons[2], and Robert Visinka[2] for the CBM-Collaboration — [1]KIT, 76344 Eggenstein-Leopoldshafen, Deutschland — [2]GSI, 64291 Darmstadt, Deutschland

The double-sided silicon microstrip sensors of the Silicon Tracking System (STS) of the Compressed Baryonic Matter (CBM) experiment at FAIR, GSI are connected to the read-out electronics by low mass flexible microcables due to tight material budget restrictions. The cable length of up to 50 cm and its flexible nature make detector module assembly one of the most critical parts in STS. The established interconnection technology for the modules is aluminum - aluminum TAB bonding. While the TAB bonding technology provides a reliable interconnection between cable and die, the module production will be a highly manual and thus time-consuming procedure. Therefore, an additional interconnection technology is being developed based on a double-layered copper microcable. This microcable allows for a novel flip-chip detector production method based on high-density gold-stud bumping on the silicon die and fine-grain solder paste printing on the microcable. We present both the TAB bonding and the novel flip-chip production method together with the design and characterization of the developed copper microcable.

HK 8.5 Mo 15:00 HS 12

A new Fault Tolerant Local Monitoring Control Board with SEU mitigation and execution redundancy commercial micro-controller — •Jose Antonio Lucio Martinez and Udo Kebschull for the CBM-Collaboration — IRI Goethe Universität Frankfurt, Frankfurt am Main, Germany

Since reliable program execution is necessary for the experiment integrity, new Fault Tolerant Local Monitoring Control (FTLMC) board for high energy particle detectors was developed to operate in harsh environments, taking into account the challenges that high energy physics experiments represent, a Commercial Off the Shelf (COTS) Micro Controller (MC), previously tested in accelerated particle beam, was populated in such board. The MC is the TMS570 conceived for safety and critical applications. The FTLMC provide the necessary interfaces such as SPI, I2C, CAN bus and others for detector parameter surveillance in experimental physics applications. Experimental Physics and Industrial Control System (EPICS), a commonly used SCADA for physics experiments, is ported to the MC where pre-built specific mechanisms are used to apply redundancy to programs executing with insignificant amount of CPU overhead.

HK 8.6 Mo 15:15 HS 12

High-Level Synthesis in Algorithm Implementation and Data Preprocessing on FPGAs — •Thomas Janson and Udo Kebschull — IRI, Goethe-Universität Frankfurt am Main, Senckenberganlage 31, 60325 Frankfurt am Main, Germany

In this talk, we discuss the high-level synthesis methodology from Xilinx to implement algorithms on FPGAs. The idea is to use a C++ high-level language to program an algorithm for an implementation in a massive parallel fashion, where we start from a data dependency analysis and define a data dependency graph with the goal to get a deeply pipelined implementation. In this approach, the challenge is the distribution of local on-chip memory close to the implemented arithmetic blocks in such a pipelined fashion. We compare this with an implementation using a data-flow programming approach like MaxJ from Maxeler, where an algorithm is described as a synchronous data-flow graph and implemented as a deep pipeline. In addition, we discuss the local memory distribution using the Maxeler data-flow approach compared to the Xilinx HLS approach.

HK 8.7 Mo 15:30 HS 12

Evaluation of High-Level Synthesis Approaches for FPGA-based Data Processing Algorithms — •Heiko Engel and Udo Kebschull for the ALICE-Collaboration — IRI, Goethe-Universität Frankfurt a. M.

The ALICE experiment uses an FPGA-based cluster finding algorithm implemented in the readout board to pre-process experimental data on the fly. This cluster finding algorithm, as used for the processing of raw TPC data during Run1 and Run2, saved significant amounts of CPU power in the HLT cluster and was a central part of the HLT data compression and reconstruction scheme. A similar concept is prepared for the ALICE readout for Run3. FPGA-based data processing steps are typically described in low-level hardware description languages like VHDL or Verilog, which come with considerable costs to develop, verify and maintain the hardware implementation. High-level synthesis

approaches promise to ease the development of data processing steps in hardware. This contribution shows approaches and results of implementing the algorithmic hardware processing steps with high-level synthesis tools on the example of the Run2 hardware cluster finder and evaluates HLS use cases for future applications.

HK 8.8 Mo 15:45 HS 12

Ladder assembly procedure for the Silicon Tracking System of the CBM Experiment — •Shaifali Mehta for the CBM-Collaboration — Universität Tübingen, Tübingen, Germany — GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany

The Compressed Baryonic Matter (CBM) experiment is one of the major scientific pillars of the future Facility for Anti-proton and Ion Research (FAIR), which is presently under construction adjacent to GSI, Darmstadt. In the CBM experiment, the main task of the Silicon Tracking System is to reconstruct the tracks and measure the momentum of charged particles. The detector comprises of 896 detector modules, based on double-sided silicon microstrip sensors distributed on 8 tracking stations. The stations are made from mechanical half units onto which carbon fibre detector ladders are mounted holding the modules. A tool has been designed to study the feasibility of the ladder assembly. One half of the longest ladder variant has been assembled with 5 non-functional modules. The same assembly technique was used to build a ladder with two functional modules for the mini-STS detector demonstrator which is currently in the mini-CBM set-up at SIS18.

This work focuses on integrating modules onto ladders which are then optically surveyed with a precision of ± 10 μm. The ladder assembly concept of mounting the modules on the ladder with a mechanical precision better than 100 μm will be presented in this talk.