HK 40: Instrumentation IX

Time: Wednesday 16:30–19:15 Location: J-HS K

Group Report HK 40.1 Wed 16:30 J-HS K

Status of upgrading the HADES tracking system frontend electronics — •Christian Wendisch for the HADES-Collaboration — GSI Helmholtz-Zentrum Darmstadt

HADES is one of the running experiments for FAIR phase 0 at SIS-18 (GSI Darmstadt). It is planned to continue running until being setup in the CBM cave for SIS-100 experiments. In the course of these plans an upgrade of the 20 years old frontend electronics of the tracking system is being conducted to further imrove the sensitivity the 24 drift chambers. For the analog part the PASTREC ASIC will replace the ASD8 chips employed so far. PASTREC was originally developped for straw tubes at AGH Krakov. A series of test campaigns has meanwhile been conducted to validate this ASIC for drift chambers, recently at COSY (Jülich). This report will present the status of this project with a focus on the latest test beam results.

supported by BMBF and GSI

Group Report HK 40.2 Wed 17:00 J-HS K

An FPGA-based Sampling-ADC Readout for the Crystal Barrel Calorimeter — •Johannes Müllers for the CBELSA/TAPS-Collaboration — Helmholtz-Institut für Strahlen- und Kernphysik, Bonn

The CBELSA/TAPS experiment at the electron accelerator ELSA (Bonn) investigates the photoproduction of mesons off protons and neutrons. After a redesign of the front-end and back-end electronics of the Crystal Barrel calorimeter, the experiment is taking data again since 2017.

One component remains to be exchanged: The charge-sensitive digitizer (QDC) of the calorimeter. It limits the readout rate of the experiment to 2kHz and cannot detect pile-up events in the high-rate forward angles. A new sampling-ADC has been adapted from the PANDA-SADC as a replacement for the QDC, featuring 14bit@80MS/s ADCs and Kintex 7 FPGAs. A custom firmware allows to extract energy and timing information and can detect pile-up pulses. The firmware has been tested with event rates well above 10kHz and delivers data reliably over a 1Gbit/s UDP link.

The sampling-ADCs have been running in a prototype setup in parallel to the QDC readout for multiple beam times, with one quarter of the calorimeter read out. The hardware development will be summarized and selected modules and algorithms of the firmware will be presented. The performance will be demonstrated with various analysis results.

HK 40.3 Wed 17:30 J-HS K

The front-end signal path of the P2 experiment at MESA — Sebastian Baunack[1], Michael Gericke[3], Kathrin Imai[1], •Rahima Krini[1], Werner Lauth[1], Frank Maas[1,2], David Rodriguez Pineiro[2], and Malte Wilfert[1] — [1]Institute for Nuclear Physics, Mainz, Germany — [2]Helmholtz Institute Mainz, Germany — [3]University of Manitoba, Canada

The MESA accelerator will be built in the Institute for Nuclear Physics in Mainz. In this facility the parity-violating asymmetry of the elastic electron-proton scattering will be measured with high precision at the P2 experiment, in order to determine the weak mixing angle $\sin^2_{eff}(\theta)$. Therefore, many technical challenges have to be solved.

The small asymmetries $\mathcal{O}(10^{-8})$ and the high precision require very high statistics and therefore a long measurement time. A joint readout electronics for P2 experiment in Mainz and for Moeller experiment at the Jefferson Laboratory is under development by collaborators of University of Manitoba. The challenge is to control the integrating detector signal chain and all sources of electronics noise within the whole experimental P2 set-up. A first prototype was build and tested at MAMI (Mainzer Mikrotron).

HK 40.4 Wed 17:45 J-HS K

Status and development of FEBs for the CBM-TRD — •Florian Roether for the CBM-Collaboration — Institut für Kernphysik, Frankfurt am Main

The Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) will explore the QCD phase-diagram in the region of high net-baryon densities. The Transition Radiation Detector (TRD) with its multi-layer-design will provide electron identification and contribute to particle tracking as well as the identification of light nuclei.

The detector signals will be digitized by the Self-triggered Pulse Amplification and Digitization ASIC (SPADIC), collected by the GBTx based Readout Board (ROB) and pre-processed by the Data Processing Board (DPB).

Therefore, the SPADIC is the key component in the TRD Front End Electronic (FEE). This talk will focus on the current status and development of the corresponding Front End Boards (FEBs) for the TRD and on test results from a recent beam test at DESY.

This work is supported by BMBF-grant 05P15RFFC1 and 05P19RFFC1.

HK 40.5 Wed 18:00 J-HS K

Particle detection with Arduino-based readout electronics — •Markus Köhli[1,2], Jannis Weimar[1], Fabian Allmendinger[1], Fabian Schmidt[2], Jochen Kaminski[2], Klaus Desch[2], and Ulrich Schmidt[1] — [1]Physikalisches Institut, Heidelberg University, Germany — [2]Physikalisches Institut, University of Bonn, Germany

Open Hardware-based microcontrollers, especially the Arduino platform, have become a comparably easy-to-use tool for rapid prototyping and implementing creative solutions. Such devices in combination with dedicated frontend electronics can offer low cost alternatives for student projects and independently operating small scale instrumentation. Clocked at 8-96 MHz, the capabilities can be extended to data taking and signal analysis at decent rates. We present two projects, which cover the readout of proportional counter tubes and of scintillators or wavelength shifting fibers with Silicon Photomultipliers. With the SiPMTrigger we have realized a small-scale design for SiPMs as a trigger or veto detector. It consists of a custom mixed signal frontend board featuring signal amplification, discrimination and a coincidence unit for rates up to 200 kHz. The nCatcher board transforms an Aruino Nano to a proportional counter readout with pulse analysis - time over threshold measurement and a 10-bit analog-to-digital converter for pulse heights. The device is therefore suitable for low to medium rate environments, where a good signal to noise ratio is crucial - in case presented here to monitor thermal neutrons.

HK 40.6 Wed 18:15 J-HS K

A Controller for the Crystal Barrel Sampling ADCs — •Knaust Jens and Müllers Johannes for the CBELSA/TAPS-Collaboration — Helmholtz-Institut für Strahlen- und Kernphysik, Bonn, Germany

The CBELSA/TAPS experiment at the accelerator ELSA (Bonn) performs photo-induced baryon spectroscopy. For the readout of the Crystal Barrel calorimeter, a new generation of data acquisition modules (Sampling ADCs) has been developed. Whilst these send the acquired event data directly via an Ethernet link, they rely on further interfaces for operation.

The controller designed and presented in this talk integrates the SADCs into the setup of the CBELSA/TAPS experiment. It supplies the experiment's trigger and synchronization logic, and access for a monitoring and control interface. For debugging and programming purposes, it is also possible to remotely access the JTAG interface of the modules.

The design's central control element is a Xilinx Zynq, which fuses a processor with an FPGA. This combines the advantages of both systems and is used to implement the remote JTAG interface as well as a convenient control interface. This browser based interface allows monitoring of all modules as well as more advanced tasks like reprogramming of their firmware.

The talk will present aspects of the hardware design such as the implementation of the remote JTAG implementation (Xilinx Virtual Cable) in the Linux subsystem.

HK 40.7 Wed 18:30 J-HS K

A Sampling ADC-readout for the Crystal Barrel Calorimeter - Digital Filtering and Deconvolution, Pile-Up Detection and Recovery — •Jan Schultes for the CBELSA/TAPS-Collaboration — HISKP, Universität Bonn

The Crystal Barrel Calorimeter consists of 1320 CsI(Tl) scintillating

crystals, which are read out by Avalanche-Photo-Diodes after a recent upgrade. As first step of a further upgrade and since those have to cope with the highest rates, the signals of the forward part of the detector are now digitized by FPGA-controlled Sampling ADCs. This offers new possibilities to detect pile-up and perform pile-up recovery, thus allowing to reach even higher rates without a loss of data quality in the main calorimeter. It has been shown that it is possible to detect pile-up events with high sensitivity using the new setup. Results of the subsequent pile-up correction as well as its impact on data analysis are presented alongside the discussion of specifically developed methods in digital signal processing, filtering and deconvolution.

HK 40.8 Wed 18:45 J-HS K

The CBM-TRD Data Processing Board Firmware — •David Schmidt for the CBM-Collaboration — Infrastructure and Computer Systems in Data Processing, Frankfurt, Deutschland

The Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany, is a fixed target heavy-ion physics experiment. The goal of the experiment is to probe the QCD phase diagram at very high net-baryon densities and moderate temperatures. The SIS-100 accelerator will provide a high luminosity heavy-ion beam, which allows for the measurement of particles with very low production cross sections. CBM is designed without a hierarchical trigger system, therefore self-triggered radiation hard readout electronics are required to cope with interaction rates of up to 10 MHz. The Transition Radiation Detector (TRD) employs the SPADIC 2.2 as the readout ASIC, featuring 32 channels and two GBTx e-links. The timestamped hit messages from the SPADIC have to be processed in the TRD-DPB (Data Processing Board) to be compatible with the CBM microslice readout. A microslice contains all the self-contained data in a given timeframe from a detector sub-system. An overview of the TRD-DPB firmware and in particular the data processing will be given.

This work is supported by BMBF-grants 05P15RFFC1 and 05P19RFFC1.

HK 40.9 Wed 19:00 J-HS K

A sampling ADC system for front end free straw tubes readout — •Paweł Kulessa[1], Andreas Erven[1], Tanja Hahnraths von der Gracht[1], Lioubov Jokhovets[1], Henner Ohm[1], Krzysztof Pysz[2], Jim Ritman[1], Christian Roth[1], Mario Schlösser[1], Thomas Sefzick[1], Valery Serdyuk[1], Stefan van Waasen[1], and Peter Wintz[1] — [1]FZJ Jülich, Germany — [2]INP PAN Kraków, Poland

Tracking systems consisting of several thousand straw tubes are forseen for the FAIR experiments. A readout must run in a triggerless mode at an average rate up to 1 MHz per straw and has to provide both time and energy loss information for particle tracking and identification. The standard readout scheme of such systems is to place front end electronics inside the detector and a free-running TDC readout outside.

This talk presents a sampling ADC (sADC) system, which has no electronic parts inside the detector, consequently no heating problems exist, no radiation damage can happen, the granularity of the system is very high and the space needed inside the detector is reduced.

The sADC system consists of: coaxial cables, HV decoupling boards in dedicated crates, preamplifiers and 250 MHz sADC boards placed in two openVPX crates. Per crate 14 sADC and preamplifiers (160 channels each), one data concentrator and one controller boards are foreseen. The FPGA (VIRTEX7) firmware provide: pulse and pile-up detection, baseline determination and correction, extraction of signals time and charge information. It can also provide other information e.g. signal amplitude, time over threshold or the "raw" signal shape.