T 104: DAQ, trigger and electronics V

Time: Friday 11:00–12:30 Location: L-3.015

T 104.1 Fri 11:00 L-3.015

Closing status of the Fast TracKer system — •Marta Czurylo and André Schöning for the ATLAS-Collaboration — Heidelberg Universität, Germany

The Fast TracKer (FTK) system for the ATLAS detector is presented. FTK was a system designed to process hits of the silicon Inner Detector (ID), and to provide full tracking information at the High Level Trigger on events first accepted at the Level-1 trigger. FTK should have allowed to significantly reduce the computing load necessary to perform tracking over the full ID volume compared to the CPU-based tracking.

Progress achieved during the LHC Long Shutdown 2 (LS2) including the hardware and software status of the system at the time of closure as well as the most recent tracking performance analysis based on the collected data from the partially running system will be discussed. Experience from the FTK project provided important input to the design of the new "Hardware Tracking for the Trigger" project, an FTK follow up project for the High-Luminosity LHC.

T 104.2 Fri 11:15 L-3.015

Online data reduction with FPGA-based track reconstruction for the Belle II DEPFET Pixel Detector — •Bruno Deschamps, Christian Weseel, and Jochen Dingfelder for the Belle II-Collaboration — University of Bonn

The innermost two layers of the Belle II vertex detector at the KEK facility in Tsukuba, Japan, will be covered by high-granularity DEPFET pixel sensors (PXD). The large number of pixels leads to a maximum data rate of 256 Gbps, which has to be significantly reduced by the Data Acquisition System. For the data reduction the hit information of the surrounding Silicon strip Vertex Detector (SVD) is utilized to define so-called Regions of Interest (ROI). Only hit information of the pixels located inside these ROIs are saved. The ROIs for the PXD are computed by reconstructing track segments from SVD data and extrapolating them to the PXD. The goal is to achieve a data reduction of up to a factor of 10 with this ROI selection. All the necessary processing stages, the receiving, decoding and multiplexing of SVD data on 52 optical fibers, the track reconstruction and the definition of the ROIs is be performed by the Data Acquisition Tracking and Concentrator Online Node (DATCON). The planned hardware design is based on a distributed set of Advanced Mezzanine Cards (AMC) each equipped with a Field Programmable Gate Array (FPGA). In this talk, the recent PHASE3 results as well as the future plans are presented.

T 104.3 Fri 11:30 L-3.015

Hard- und Firmware Entwicklung für Trigger-Module des ATLAS Level-1 Kalorimeter-Triggers — Volker Büscher, Johannes Damp, •Christian Kahra, Ulrich Schäfer, Ren-Jie Wang und Marcel Weirich — Inst. für Physik, Universität Mainz

Während dem Long Shutdown 2 (LS2) des Large Hadron Colliders (LHC), wird nicht nur der Beschleuniger ausgebaut, sondern zeitgleich auch die Triggersysteme der Experimente modernisiert, um trotz der höheren Ereignisrate weiterhin sensitiv für seltene Prozesse zu sein. Die Universität Mainz ist mit zwei Projekten am Upgrade des ATLAS Level-1 Kalorimeter Trigger beteiligt: dem *jet Feature Extractor* (jFEX) und dem *Level-1 Topologischen Prozessor* (L1Topo). Beide Projekte basieren auf gemeinsamen Hard- und Firmware-Designs, welche in diesem Vortrag vorgestellt werden.

Die Hardware-Module bieten eine Bandbreite von bis zu 3.1 *Tbps* für die Eingangsdaten, welche in Echtzeit von den Prozessor-FPGAs verarbeitet werden. Die Hochgeschwindigkeits-Datenleitungen wie auch der hohe Leistungsbedarf der FPGAs stellten hohe Anforderungen an das Design. Die Entwicklung dieser dichtbestückten Leiterplatinen, deren Simulationen und die Test-Ergebnisse der produzierten Module werden präsentiert.

Die Infrastruktur-Firmware der Prozessor-FPGAs wurde zur Nutzung in beiden Projekten generisch entwickelt. Daher ist sie auch für andere Projekte leicht anpassbar und stellt somit eine allgemein nutzbare Low-Level Abstrahierung für Echtzeit-Datenverarbeitung in FPGAs dar.

T 104.4 Fri 11:45 L-3.015

Software development for the ITk-Pixel module read-out and test system "BDAQ" — •Rafael Gonçalves Gama, Ali Skaf, Jörn Grosse-Knetter, Jörn Lange, and Arnulf Quadt — II. Physikalisches Institut, Georg-August-Universität Göttingen

The Inner Tracker (ITk) is a new all-silicon detector which will replace the current ATLAS tracking system during the Phase II upgrade. The ITk innermost layers are composed by pixel modules, which comprise a new sensor and a new front-end chip, designed to cope with the challenging demands of the HL-LHC environment. This work consists of adding support for the BDAQ hardware platform to the official ITk DAQ system, enabling the use of the said hardware in a centralized environment for the verification of pixel modules during the prototyping and (pre-)production phase of the ATLAS ITk upgrade. The BDAQ hardware is an, affordable yet powerful, FPGA-based electronics board designed by the University of Bonn for the readout of the RD53A front-end and upcoming generation chips. A new software library, based on the original BDAQ software package, was written to allow the new hardware integration into the ITk DAQ software. A summary of the development process, as well as results of the BDAQ hardware integration compared with results from the ITk software running with one of its originally supported hardware platforms, will be presented.

T 104.5 Fri 12:00 L-3.015

Echtzeit-Pfad des Tile Rear Extension (TREX) Moduls — •Damir Rassloff für die ATLAS-Kollaboration — Kirchhoff-Institut für Physik, Heidelberg

Im Zuge des Phase-I Upgrades des Atlas Experimentes steht auch der Atlas Level-1 Kalorimeter Trigger vor einer Reihe von Upgrades. Dabei soll die hohe Effizienz der Triggerentscheidungen beibehalten werden, weshalb drei neue digitale Indentifizierungsprozessoren verwendet werden. Die Prozessoren erhalten aus dem LAr-Kalorimeter digitalisierte Daten bei erhöhter Kalorimetergranularität. Das Tile-Kalorimeter hingegen wird weiterhin analoge Daten an das L1Calo Preprozessor System senden, welche dort digitalisiert werden. Die digitalisierten Daten werden daraufhin mit Hilfe der Tile Rear Extension (TREX) Module formatiert und an die neuen Prozessoren über optische Verbindungen weitergeleitet. Die verwendeten TREX Module sind komplexe PCBs, mit hochmodernen FPGAs und Hochgeschwindigkeitstransceivern.
Zur Zeit befindet sich das neue Atlas Level-1 Kalorimeter Trigger System innerhalb eines selbstständigen Teststandes unter ausführlichen Tests, in denen auch der zuvor beschriebene Echtzeitpfad validiert wird. Das Hauptaugenmerk dieses Vortrages soll auf den Untersuchungen des Echtzeitpfades liegen und dabei vor allem die Kommunikation zwischen der TREX Module und den neuen Indentifizierungsprozessoren betrachten. Zum besseren Verständnis wird zuvor ein Überblick des Atlas Level-1 Kalorimeter Trigger Grundsystems sowie des TREX Moduls gegeben.

T 104.6 Fri 12:15 L-3.015

Prototyping Serial Powering with RD53A — •Florian Hinterkeuser, Matthias Hamer, Hans Krüger, Fabian Hügging, and Klaus Desch for the ATLAS-Collaboration — Universität Bonn

The high luminosity upgrade for the Large Hadron Collider at CERN requires a complete overhaul of the current inner detectors of ATLAS and CMS. These new inner detectors will consist of all-silicon tracking detectors. A serial powering scheme has been chosen as baseline for the pixel detector to cope with the higher number of modules and the higher power consumption of the new front-end chip, spatial constraints and the need to minimalize the tracker's material budget. This new powering scheme provides challenges for the electrical and mechanical design. In order to verify this new powering scheme and its implications on the detector integration, efforts are ongoing to set up a prototype for serial powering using modules based on the RD53A chip, a half-size prototype for the new Pixel front-end chip, developed by the RD53 collaboration. In particular, a serial powering stave consisting of up to 8 RD53A quad chip modules has been set up in Bonn. First results from the ongoing activities with RD53A chips are presented. Emphasis is put on the electrical characterization of a RD53A serial powering chains, using representative services and power supplies. The setup, measurement goals and characterization of the serial powering chain and recent R&D activities focused on serial powering components will be discussed.