T 31: Pixel detectors II

Time: Tuesday 17:00–18:35 Location: H-HS XIV

Group Report T 31.1 Tue 17:00 H-HS XIV

Overview of depleted monolithic active pixel sensors in the LFoundry 150 nm and TowerJazz 180 nm CMOS technologies — •Tianyang Wang and Konstantinos Moustakas — Physikalisches Institut, University of Bonn, Germany

CMOS pixel sensors utilizing commercial processes have already been used in high energy particle physics experiments for high precision charged particle tracking. They integrate sensing elements and electronics on the same silicon substrate and can offer lower material budget, lower cost and easier module assembly as compared to the hybrid pixels where the sensing and electronic parts are different entities mated with the cost intensive bump-bonding technology. However, the existing mature CMOS devices cannot withstand the high particle rate and high radiation environments encountered, for example, at the future HL-LHC, with the main limiting factor being the predominant diffusion movement for charge collection. We have been developing CMOS pixels with greatly enhanced radiation tolerance and timing precision for many years. The key ingredient for such sensors is a fully depleted sensing volume that allows for fast charge collection in a strong drift field. We have focused recently on two development lines, pursuing two different sensor design concepts in the LFoundry 150 nm and TowerJazz 180 nm CMOS technologies respectively. Large-scale demonstrator chips incorporating a fast readout architecture have been designed and characterized in both technologies. In this contribution, an overview of R&D activities for CMOS pixels in the aforementioned technologies will be presented.

T 31.2 Tue 17:20 H-HS XIV

Improving Spatial Resolution of Silicon Pixel Detectors through Sub-pixel Cross-coupling — •Sinuo Zhang, David-Leon Pohl, Tomasz Hemperek, and Jochen Dingfelder — Physikalisches Institute, University of Bonn, Nussallee 12, 53115 Bonn

We present a concept to improve the spatial resolution of silicon pixel-detectors via the implementation of position dependent inter-pixel cross-coupling. By segmenting the readout implantations and AC-coupling the sub-pixels, a part of the pixel charge is shared with neighboring pixels. For example, such a sensor can be realized in radiation tolerant high-voltage CMOS processes facilitating its application in modern particle colliders. Simulations to study the impact of different coupling capacitances on the spatial resolution are presented and an improvement of the spatial resolution by approximately 40% is demonstrated.

T 31.3 Tue 17:35 H-HS XIV

Active pixel sensor with small pixel size designed for capacitive readout with RD53 ASIC — •Hui Zhang — Karlsruher Institut für Technologie

We are designing HVCMOS sensors for several particle physics experiments. These sensors are simple and low cost alternative to classical hybrid detectors. HVCMOS sensor can either contain readout circuits on chip (monolithic sensors) or they can be readout by an external readout ASIC by means of capacitive signal transmission (capacitively coupled hybrid particle detector - CCPD). Both approaches have certain advantages. The detector chip for a CCPD has been implemented in an 180nm HVCMOS process. Depleted high voltage n-well/p-substrate diodes are used as sensors. Every pixel has a size of 25μm x 50μm and contains a charge sensitive amplifier and a simple comparator. The outputs of two pixel comparators are connected to a transmitting electrode (pitch 50μm x 50μm) implemented in the top metal layer of the sensor chip. A process modification has been done specially for this chip – deep p allows implementation of comparators in pixel. The readout chip and the sensor chip can be mechanically connected either by glue (standard option) or as a novel approach with a small number of large bump bonds. The output signals of the sensor chip are transmitted capacitively to the input pads of the readout chip which are connected to the signal receivers. The sensor chip has been produced and tested. Parameters such as amplitude, pulse width, rise time and signal noise ratio have been measured. In this talk, the sensor design and the measurement results will be presented.

T 31.4 Tue 17:50 H-HS XIV

Monolithic Pixel Sensors with sub-nanosecond time resolution in BiCMOS — Heiko Augustin[1], Ivan Peric[2], André Schöning[1], and •Benjamin Weinläder[1] — [1]Physikalisches Institut, Heidelberg, Germany — [2]Karlsruher Institut für Technologie, Germany

In recent years, the development of High Voltage Monolithic Active Pixel Sensors (HV-MAPS) has been strongly driven forward. As an example of the latest successes, the MuPix8 can be mentioned, which reached a time resolution of $\sigma_t = 6.8 \pm 0.2$ ns.

The combination of HV-MAPS with a BiCMOS technology opens up further possibilities, especially for the improvement of the time resolution. At the University of Geneva a time resolution of $\sigma_t = 46 \pm 2$ ps has been achieved for a small prototype sensor based on BiCMOS.

According to this concept and based on the experience from the MuPix development a new R&D project was started , with the ambition to achieve a time resolution below 1 ns over a large pixel matrix. For this project the BiCMOS technology SG13S from IHP is used, which offers great advantages for high-frequency circuits. Therefore, the analogue circuits inside the pixel will be redesigned, making use of the bipolar technology. The concept here is to use a plain bipolar amplifier in order to decrease the noise from various components and the rise time of the signal edge. Simulations with Cadence Virtuoso® are done to investigate the performance of BiCMOS technology and to make a prediction about the time resolution of the new read-out tree.

T 31.5 Tue 18:05 H-HS XIV

Development of the next generation of high speed hybrid pixel detectors for the European Center of Nuclear Research (HL-LHC) — •Mark Standke, Michael Daas, Yannick Dieter, Piotr Rymaszewski, Markus Frohne, Tomasz Hemperek, Hans Krüger, David-Leon Pohl, Marco Vogt, Norbert Wermes, and Jochen Dingfelder — Physikalisches Institut der Universität Bonn

The European Center for Nuclear research (CERN) in Geneva Switzerland is increasing the luminosity of its Large Hadron Collider in 2026 (HL-LHC). Higher Luminosity leads to new challenges regarding spacial resolution, readout speed and radiation hardness for the tracking detectors at the HL-LHC. Especially detectors in the vicinity to the particle interaction point face significantly higher particle intensities. For this challenging task ATLAS and CMS have joined forces to develop a new, high resolution, high speed, and high radiation resistant readout chip for their hybrid pixel detectors. This talk will give an overview of past, present and future developments of this next generation of hybrid pixel detector readout chips and focus on the development status of their most recent chip iteration called RD53B.

T 31.6 Tue 18:20 H-HS XIV

Bump bond stress tests with ITk-Pixel-style daisy-chain and FE-I4-modules through thermal cycling — •Steffen Korn, Jörn Grosse-Knetter, Jörn Lange, and Arnulf Quadt — II. Physikalisches Institut, Georg-August-Universität Göttingen

Early module prototypes for the new ATLAS Inner Tracker Pixel Detector (ITk) highlighted bump bond connections as a possible point of failure in future ITk Pixel modules when exposed to thermally induced stress. In order to investigate this issue, daisy chain modules with realistic bump bond pitch and modules with read-out-chips were tested before, during, and after exposure to thermal stress through cycling in a thermal shock chamber in Goettingen. The results of these tests using different modules with different assembly options are presented in this talk.