T 40: DAQ, trigger and electronics II

Time: Tuesday 17:00–18:30 Location: L-3.015

T 40.1 Tue 17:00 L-3.015

Developement of automated quality tests for the RD51 VMM3a Hybrid — •Finn Jaekel, Jochen Kaminski, Michael Lupberger, and Patrick Schwäbig — Physikalisches Institut, Universität Bonn

The Scalable Readout System of the RD51 Collaboration is a diverse readout system, which is used in many areas in the developement of gaseous detectors. It supports different front-end chips like Timepix, VFAT or APV25 and contains the complete readout-chain to transfer data between the detector and the computer. Until recently the APV25 ASIC was frequently used. As nowadays it is not produced anymore, a new front end chip - the VMM ASIC (developed for the ATLAS New Small Wheels upgrade) - was developed and integrated into the scalable readout system.

The project currently is on its way from developement to mass production. There is already strong interest to use the readout system for a wide variety of experiments and research projects. Especially the front-end printed circuit board with the VMM chip, called hybrid, of which large amounts will be produced, requires automated quality assurance.

In this talk quality criteria, developement of an automated testing procedure, as well as first results of these quality tests will be presented.

T 40.2 Tue 17:15 L-3.015

Development of Calibration Procedures for NSW Micromegas readout electronics — •Vladislavs Plesanovs, Stephanie Zimmerman, and Gregor Herten — Albert-Ludwigs-Universität Freiburg, Freiburg im Breisgau, Germany

During the current LS2 at CERN, ATLAS muon spectrometer will be upgraded by exchanging one of its inner end-caps. The aim is to have an extra input to the L1 muon trigger system to cope with expected event rate and to lower fake-muon trigger rate significantly. For this purpose the New Small Wheel (NSW) will consist of two complementary detector technologies: sTGC (trigger) and MicroMegas (tracking). Data readout from these detectors will be conducted by dedicated front-end electronics.

Before physics data taking, a calibration of the readout electronics and signal conversion from digital units to physical values is required. Calibration procedure sets a global threshold above the noise on the readout chip level and adjusts it individually for each of $\approx$ 2 million channels. Second part requires a conversion procedure of the input charge from ADC counts to Coulombs and time from bunch crossing clock units to nanoseconds for further data processing.

This presentation will discuss how the developed procedures are integrated with cutting-edge technologies like FELIX, ALTI and present ATLAS TDAQ infrastructure. Also, challenges that were tackled at the development stage together with calibration results of the first commissioned sector of the NSW will be presented.

T 40.3 Tue 17:30 L-3.015

Redevelopment of RawDataAnalysis package for ATLAS pixel detector — •Buddhadeb Mondal[1], Oldrich Kepka[2], Carmen Diez Pardos[1], and Ivor Fleck[1] for the ATLAS-Collaboration — [1]University of Siegen, Siegen, Germany — [2]Institute of Physics, Prague

The RawDataAnalysis package is a part of the ATLAS pixel DAQ (Data Acquisition) infrastructure used for analyzing ATLAS raw data for commissioning the pixel and IBL detectors. The package comprises a decoder and an analysis framework. The decoder takes the raw data as input, decompresses it and it reads pixel and IBL ROB (readout buffer) fragments. Then it decodes the encrypted DAQ logic information from the data and stores it as ROOT object tree. An analysis framework enables access to the decoded ROOT tree and provides common functionality for further analysis.

This tool offers full information about the raw data, low-level validation of DAQ logic and reconstruction chain, ROD (readout driver)/Module error analyses, hit-level occupancy counting, ToT (time over threshold) measurement, timing information at the pixel level, validation of data quality monitoring plots and it can be used for other detector related studies. In this talk development of this package and how this package is used in the ATLAS pixel group will be presented.

T 40.4 Tue 17:45 L-3.015

Firmware development for the Scalable Readout System (SRS) with VMM3a — •Patrick Schwäbig, Finn Jaekel, Jochen Kaminski, and Michael Lupberger — Physikalisches Institut, Universität Bonn

The Scalable Readout System which was developed within the RD51 collaboration is a flexible readout system which can be used with various front-end chips and is scalable from a few channels to many thousand channels.

As a future-oriented technology the VMM front-end chip (ASIC) has been chosen as a successor for the so far mainly used APV25 for innovations in gaseous detector development. Originally developed for the New Small Wheel Upgrade of the ATLAS detector the VMM offers features like continuous readout, which are required to fulfill future demands e.g. for use in the NMX instrument at the European Spallation Source (ESS).

The VMM ASIC has been implemented in recent years in the SRS and was tested in various projects. Additional improvements and enhancements are in ongoing development.

The talk will focus on the progression of the firmware of the FPGA responsible for the VMM readout. Improvements of readout reliability and readout speed as well as future plans will be presented.

T 40.5 Tue 18:00 L-3.015

DC-DC converter for powering the Mu3e detector — •Sophie Gagneur[1], Thomas Rudzki[2], Frederik Wauters[1], and Niklaus Berger[1] for the Mu3e-Collaboration — [1]Institut für Kernphysik Johannes Gutenber-Universität, Mainz — [2]Physikalisches Institut Heidelberg

The Mu3e experiment under construction at the Paul Scherrer Institute, Switzerland, aims to measure the lepton flavour violating decay of a muon into one electron and two positrons with an ultimate sensitivity of one in 10^{16} muon decays.

The detector for the Mu3e experiment consists of High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) combined with scintillating tiles and fibres. The detector ASICs need a supply voltage of around 2 V. This voltage is going to be generated from the 20 V external supply via DC-DC converters. These buck converters must be able to operate within a magnetic field and provide a constant output voltage with a ripple of less than 10 mV to guarantee a proper operation of the pixel sensors and timing detectors. This will be achieved by the use of custom air coils, the implementation of additional output filters and an optimized PCB design. The first version of the converter has been successfully tested with the MuPix8 prototype pixel sensor.

T 40.6 Tue 18:15 L-3.015

Evaluation einer neuen Netzwerk-Technik für die Detektor-Auslese — •Carsten Dülsen, Tobias Flick, Wolfgang Wagner und Marius Wensing — Bergische Universität Wuppertal

Für die Übertragung von Auslesedaten vom FPGA zur Software wird ein Ansatz vorgestellt, bei dem die Daten über ein herkömmliches Netzwerk (UDP/IP) versendet werden. Dabei wird versucht den Datenverlust soweit zu reduzieren, dass die Auslese auch ohne Speicherung und erneutes Versenden der Daten auskommt. Dazu wird eine eXpress Data Path (XDP) genannte Technik untersucht und ihre Eignung im Umfeld des ATLAS ITk Pixel Detektors getestet.