T 86: DAQ, trigger and electronics IV

Time: Thursday 16:30–18:30 Location: L-3.015

T 86.1 Thu 16:30 L-3.015

Design of the Event Builder for the OSIRIS pre-detector of JUNO — •Runxuan Liu[1,2], Christoph Genster[1], Kai Loo[4], Livia Ludhova[1,2], Alexandre Göttel[1,2], Yu Xu[1,2], Yuhang Guo[1,3], Philipp Kampmann[1,2], Giulio Settanta[1], and Cornelius Vollbrecht[1,2] — [1]Institut für Kernphysik, Forschungszentrum Jülich, Jülich 52428, Germany — [2]III. Physikalisches Institut B, RWTH Aachen University — [3]School of Nuclear Science and Technology, Xi'an Jiaotong University, Xi'an 710049, China — [4]Johannes Gutenberg-University Mainz, Institute of Physics, 55128 Mainz, Germany

JUNO is a 20 kt liquid scintillator detector under construction in Jiangmen, China, whose goal will be to determine the neutrino mass hierarchy. In order to meet the stringent requirements on the radiopurity of the liquid scintillator, the OSIRIS pre-detector is being designed to monitor the liquid scintillator during the several months of filling the large volume of JUNO. OSIRIS will contain 20 ton of scintillator and will be equipped with 76 20-inch PMTs. The DAQ system will have no global hardware trigger: instead, each PMT will provide a data-stream composed of the waveforms, each containing a gps time stamp. Based on the latter, dedicated offline trigger software will organize individual waveforms into events. This talk will discuss the optimization of the event builder trigger conditions, considering the expected rates of different backgrounds and the PMTs dark rate and using the OSIRIS simulation software.

T 86.2 Thu 16:45 L-3.015

Development of a tester hardware tool for new read-out electronic cards of the ATLAS muon detector monitored drift tubes for the Phase-II upgrade — •Mathias Modlmayr, Gia Khoriauli, and Raimund Ströhmer — Julius-Maximilians-Universität Würzburg

The ATLAS detector is a experiment at the Large Hadron Collider (LHC) at CERN and collects data from particle collisions with energies in the multi-TeV range. The monitored drift tubes (MDT) are a part of the ATLAS muon spectrometer and are used to identify and measure muon tracks. The MDT are read-out with on-chamber mezzanine cards which are equipped with signal amplifier-shaper-discriminator and time to digital converter chips. For the High Luminosity LHC, this front-end electronics has to be replaced with the new mezzanine cards being developed. We develop a hardware tool to test the functionality of the new mezzanine cards. Hardware and software specifications as well as the status of the development of the tool is presented.

T 86.3 Thu 17:00 L-3.015

Logging and Monitoring Architecture for the High Level Trigger at the Belle II Experiment — •Anselm Baur[1], Markus Prim[1], Takuto Kunigo[2], Pablo Goldenzweig[1], and Florian Bernlochner[3] — [1]Karlsruhe Institute of Technology, Germany — [2]KEK, Tsukuba, Japan — [3]University of Bonn, Germany

The Belle II online software trigger — the so-called High Level Trigger (HLT) — is the second and last trigger stage applied to the detector data before it is written to permanent storage. Its purpose is to select events with interesting physics signatures to reduce the data rate from the Level-1 trigger from 30 kHz to 10 kHz. The HLT design foresees $\mathcal{O}(5000)$ CPU cores distributed to $\mathcal{O}(20)$ hardware nodes. The same Belle II analysis software framework (basf2) used for offline reconstruction is running on the HLT nodes for the online reconstruction.

This architecture has to be monitored to ensure smooth processing. Therefore, all the log outputs of the system and running subsystems are bundled in a central monitoring environment. Such a central monitoring system provides fast error recognition and enables a quick identification of problematic subsystems. Additionally, detecting issues which may lead to future errors and analysing error correlations is a power of such a monitoring approach. In this talk, we present a monitoring system with Elastic Stack for the HLT at the Belle II experiment.

T 86.4 Thu 17:15 L-3.015

Development of a radiation hard ASIC to be used for the monitoring of the ATLAS ITk Pixel detector — •Rizwan Ahmad[1], Susanne Kersten[1], Christian Zeitnitz[1], Peter Kind[1], Ahmed Qamesh[1], Michael Karagounis[2], Alexander Walsemann[2], and Tobias Fröse[2] — [1]University of Wuppertal, Wuppertal, Germany — [2]University of Applied Sciences and Arts, Dortmund, Germany

For the phase II upgrade of ATLAS, a new ITK pixel detector is under development. In this context, the ATLAS pixel detector will get a new DCS (Detector Control System) which is being developed at the University of Wuppertal. The control and monitoring path of the DCS system has two main entities. The DCS computer (Main Control room) and the MoPS (Monitoring of Pixel System) chip.

The MoPS chip monitors temperature and voltages of the different sub-detector parts. The chip communicates to the DCS computer over CAN (Controller Area Network) bus. This chip has a 12-bit ADC to read up to 35 channels and it implements a part of the CANopen standard. The MoPS must be radiation hard up to an ionizing dose of $>$ 500 Mrad and it must also provide great immunity against SEU (Single Event Upsets). This chip implements a non-standard CAN physical layer with a maximum voltage of 1.2 Volt. The first prototype of the chip implements core digital functionality and all the analog components required for the operation of the chip. In this talk functionality, simulation results and status of the chip will be presented.

T 86.5 Thu 17:30 L-3.015

Readout of the Tile Rear Extension Module for the Phase-I upgrade of the ATLAS L1Calo Trigger System — •Tigran Mkrtchyan — Kirchhoff-Institut für Physik, Heidelberg

For Run 3, the ATLAS Level-1 Calorimeter Trigger (L1Calo) system is being upgraded with new subsystems, called feature extractors (FEXes). While the Liquid Argon calorimeter will send fine-granularity digital data to the FEXes, the Tile Calorimeter (TileCal) will continue to send analogue signals to the existing L1Calo Preprocessor (PPr) subsystem. In order to provide the FEXes also with digital results from the TileCal, the L1Calo PPr is being extended with new Tile Rear Extension (TREX) modules. Equipped with advanced FPGAs and high speed optical transmitters, the TREX provides digitized hadronic transverse energy (E_T) results in real-time at the LHC clock frequency to the FEX processors via optical fibers running at 11.2 Gbps and to the legacy L1Calo processors via existing 11 m long electrical cables. Additionally, for verifying the accepted trigger decision, the TREX formats and transfers event data to the DAQ system. The event data transfer is performed via a single optical link running at 9.6 Gbps to the Front-End Link Exchange (FELIX) board. The interface to the legacy readout path to the DAQ is preserved via a single optical link running at 960 Mbps in G-Link transmission mode. In this talk, the status of production, commissioning, test results of the TREX to FELIX readout path and the data formatting analysis will be presented.

T 86.6 Thu 17:45 L-3.015

The LHCb real-time analysis concept for a purely software-based trigger for Run III of the LHC — •André Günther[1], Stephanie Hansmann-Menzemer[1], Sascha Stahl[2], and Michel De Cian[3] — [1]Physikalisches Institut, Uni Heidelberg — [2]CERN — [3]École polytechnique fédérale de Lausanne

The LHCb experiment in the Run 3 environment of the LHC faces challenging rates of data containing particle decays of interest. In fact, expected signal rates alone are higher than current raw data storage capabilities. Therefore, LHCb is implementing a real-time data processing strategy and a reduced event model allowing triggering on fully reconstructed events and persisting an arbitrary set of reconstructed or raw objects. A crucial part of the real-time data analysis are fast and efficient tracking algorithms. The talk highlights ways to improve the so-called Forward Tracking, which is the algorithm reconstructing the majority of charged particle trajectories used in LHCb analyses.

T 86.7 Thu 18:00 L-3.015

Entwicklung von algorithmischer Firmware für den Ausbau des ATLAS Level-1 Jet/Energiesummen-Triggers — Volker Büscher, Christian Kahra, Ulrich Schäfer, Stefan Tapprogge und •Marcel Weirich für die ATLAS-Kollaboration — Johannes Gutenberg-Universität Mainz

In den kommenden Ausbaustufen des LHC werden immer höhere Lu-

minositäten erreicht. Dadurch werden auch immer größere Herausforderungen an das Triggersystem des ATLAS Detektors gestellt. Zusätzlich zu den steigenden Ereignisraten werden die Daten aus den elektromagnetischen und hadronischen Kalorimetern mit erhöhter Granularität übertragen. Um dies für eine effiziente Selektion von Ereignissen zu nutzen, muss das existierende System ausgebaut werden. Bei einer Datenrate von 40 MHz muss in der ersten Triggerstufe eine Entscheidung innerhalb von 2.5 μs getroffen werden.

Der jet Feature EXtractor, kurz jFEX, bildet eine Neuerung für den Ausbau des ATLAS Level-1 Triggers. Ab 2021 wird jFEX in erster Linie für die Identifikation von Jet-Kandidaten und zur Berechnung von Energiesummen eingesetzt. Pro Modul ist eine Eingangsbreite von bis zu 2.7 Tb/s erforderlich, die sich auf 4 Xilinx UltraScale+ FPGAs verteilt. Für die dort laufenden Algorithmen stehen maximal 125 ns an Berechnungszeit zur Verfügung. Aus diesem Grund müssen diese eine hochparallele Struktur aufweisen.

In diesem Vortrag wird der aktuelle Stand der Algorithmen-Implementierung vorgestellt.

T 86.8 Thu 18:15 L-3.015

Development of Digital Signal Processing for the ATLAS Liquid-Argon Calorimeters with Artificial Neural Networks using Field Programmable Gate Arrays — •Nick Fritzsche, Anne-Sophie Berthold, Rainer Hentges, Philipp Horn, and Arno Straessner — Institut für Kern- und Teilchenphysik, Dresden, Germany

The upgrade plans for the Large Hadron Collider result in more challenging requirements for the data readout of the Liquid-Argon calorimeters of the ATLAS detector. The energy deposits of particles that are formed in high-energy proton-proton collisions create electrical pulses in the detector. These undergo a digital signal processing for selecting and preparing the signals in real-time for data acquisition and trigger. In signal processing artificial neural network algorithms can be used for fast, precise and resource-saving trigger decisions and energy reconstruction. A general implementation for feed-forward networks in FPGA hardware is introduced, which is freely configurable regarding neuron number and network depth. It is capable of processing parallel as well as time-lagged inputs. Applications as optimal filters, dense and time-lagged feed-forward neural networks are presented. A simulation and an implementation for FPGAs is considered optimizing the circuit with respect to resource usage and signal delay. An efficient use of digital signal processors is realized by time division multiplexing in order to use one network for multiple input channels. Results of test runs with a slow control, which allows memory-based data injection and readout under software control, are presented.