T 20: DAQ, trigger and electronics I

Time: Monday 16:00–18:15 Location: Tt

T 20.1 Mon 16:00 Tt

Prototyping Serial Powering with RD53A — •Florian Hinterkeuser, Klaus Desch, Matthias Hamer, Fabian Hügging, Hans Krüger, and Charlotte Perry — Physikalisches Institut, Universität Bonn

The high luminosity upgrade for the Large Hadron Collider at CERN requires a complete redesign of the current inner detectors of ATLAS and CMS. These new inner detectors will consist of all-silicon tracking detectors. A serial powering scheme has been chosen as baseline for the pixel detector to cope with the higher number of modules and the higher power consumption of the new front-end chip, spatial constraints and the need to minimize the tracker's material budget.

This new powering scheme provides challenges for the electrical and mechanical design. In order to verify this new powering scheme and its implications on the detector integration, efforts are ongoing to set up a prototype for serial powering using modules based on the RD53A chip, a half-size prototype for the new Pixel front-end chip, developed by the RD53 collaboration. In particular, a serial powering stave consisting of up to 8 RD53A quad chip modules has been set up in Bonn.

First results from the ongoing activities with RD53A chips are presented. Emphasis is put on the electrical characterization of an RD53A serial powering chain, using representative services and power supplies. The setup, measurement goals and characterization of the serial powering chain will be discussed.

T 20.2 Mon 16:15 Tt

Entwicklung automatischer Qualitätstests für den RD51 VMM3a Hybrid — •Finn Jaekel, Michael Lupberger, Patrick Schwäbig und Jochen Kaminski — Physikalisches Institut Universität Bonn

Das Scalable Readout System der RD51 Kollaboration ist ein vielseitiges Auslesesystem, das in großen Bereichen der Entwicklung von gasgefüllten Detektoren verwendet wird. Es unterstützt verschiedene Front-End Chips, wie z.B. Timepix, VFAT oder APV25 und beinhaltet die komplette Auslesekette zur Übertragung von Daten zwischen Detektor und Computer. Bis vor kurzem wurde hierfür häufig der APV25 ASIC benutzt. Da dieser nun aber nicht mehr hergestellt wird, wurde ein neuer Front End Chip, der VMM (entwickelt für das ATLAS New Small Wheel upgrade)ASIC- entwickelt, in das Scalable Readout System implementiert.

Das Projekt befindet sich momentan in der Übergangsphase von der Entwicklung zur Massenproduktion. Es gibt bereits großes Interesse an dem Auslesesystem zur Verwendung für zukünftige Experimente und Forschungsprojekte. Insbesondere das Front-End board mit dem VMM chip, genannt Hybrid, von dem große Stückzahlen produziert werden, bedarf einer automatisierten Qualitätskontrolle.

In diesem Vortrag wird das im vergangenen Jahr entwickelte Testsystem vorgestellt, und erste Ergebnisse präsentiert.

T 20.3 Mon 16:30 Tt

Firmware development for the Scalable Readout System (SRS) with VMM3a — •Patrick Schwäbig, Finn Jaekel, Jochen Kaminski, and Michael Lupberger — Physikalisches Institut, Universität Bonn

The Scalable Readout System which was developed within the RD51 collaboration is a flexible readout system which can be used with various front-end chips and is scalable from a few channels to many thousand channels.

As a future-oriented technology the VMM front-end chip (ASIC) has been chosen as a successor for the so far prevailing APV25 for innovations in gaseous detector development. Originally developed for the New Small Wheel Upgrade of the ATLAS detector the VMM offers features like continuous readout, low electronic noise and neighbor-enabling logic, which are required to fulfill future demands e.g. for use in the NMX instrument at the European Spallation Source (ESS).

The VMM ASIC has been implemented in recent years in the SRS and was tested in various projects. Additional improvements and enhancements are in ongoing development.

The talk will focus on the progression of the firmware of the FPGA responsible for the VMM readout. Improvements of the readout speed and the necessary adaptions to the VMM readout process will be presented.

T 20.4 Mon 16:45 Tt

Timing Studies of KLauS6: A Low Power ASIC for Silicon Photomultiplier Charge Readout with Precise Timing — •Erik Warttman and Konrad Briggl for the CALICE-D-Collaboration — Kirchhoff-Institut für Physik, Universität Heidelberg

The scintillator-based high-granular calorimeters developed within the CALICE collaboration require sophisticated front-end readout electronics, providing precise charge and time measurements of the generated Silicon-Photomultiplier (SiPM) signals, while minimizing the power consumption. The KLauS ASIC has been developed for this application, targeting low-gain SiPMs with large dynamic range. In the recent version KLauS6, a Phase Locked Loop (PLL) driven TDC has been integrated. This enables precise time measurements with 200ps time binning. The chip has been characterized using SiPMs with and without scintillating tiles. The characterization procedures and the results from lab and testbeam measurements with a particular focus on timing will be presented.

T 20.5 Mon 17:00 Tt

Towards a Level 1 Single Track Z Trigger in the Belle II Experiment — •Felix Meggendorfer[1,3], Steffen Baehr[2], Christian Kiesling[1,4], Sebastian Skambraks[1,4], and Kai Lukas Unger[2] for the Belle II-Collaboration — [1]Max-Planck-Institut für Physik — [2]Karlsruher Institut für Technologie — [3]Technische Universität München — [4]Ludwig-Maximilians-Universität München

The Neurotrigger is a Level 1 track trigger within the drift chamber in the Belle II Experiment, which uses a neural network for the z vertex estimation. Since it ran stable in the last run period of 2020, we managed to improve the delta z resolution by using real data for the network training. We now aim for an unprescaled single track trigger operation from 2021 on. This will lead to a much better sensitivity for low multiplicity events, which is important for the discovery of new physics, for example in the sectors of tau lepton flavor violation or dark matter searches.

T 20.6 Mon 17:15 Tt

Modular and scalable Timepix3 readout system — Klaus Desch, •Markus Gruber, Thomasz Hemperek, Jochen Kaminski, Leonie Richarz, and Tobias Schiffer — Physikalisches Institut, Universität Bonn, Nußallee 12, 53115 Bonn

With the highly granular pixel ASIC Timepix3 several different detectors can be built by combining it either with a bump bonded sensor or with a photolithographically postprocessed MicroMegas gas amplification stage (InGrid). With these combinations quite different applications like beam telescopes, X-Ray detectors and neutron TPCs can be realized.

For the detectors to be built with this ASIC that range from single chip to multichip designs and from low- to high-rate applications a modular and scalable readout and control system is needed which can efficiently adapt the different scenarios. The firmware and software are based on the basil framework and as readout system several FPGA boards are supported including the Scalable Readout System (SRS) which offers scalability in low to medium rate multichip applications. Besides the capability of different detector designs the system offers optional monitoring interfaces for different detector parameters.

In this talk I will present the readout and control system and how it scales for the applications. Furthermore, I will show how the modular approach enables several different detector designs and offers the needed functionality like calibration, equalization, readout and monitoring.

T 20.7 Mon 17:30 Tt

Software trigger optimization for the OSIRIS pre-detector of JUNO — •Runxuan Liu[1,2], Philipp Kampmann[1], Kai Loo[3], Livia Ludhova[1,2], Alexandre Göttel[1,2], Mariam Rifai[1,2], Giulio Settanta[1], and Cornelius Vollbrecht[1,2] — [1]Forschungszentrum Jülich - Institute for Nuclear Physics, IKP-2, Jülich, Germany — [2]RWTH Aachen University - Physics Institute III B, Aachen, Germany — [3]Johannes Gutenberg-Universität Mainz, Institute for Physics, Staudingerweg 7, 55128 Mainz

JUNO is a 20 kt liquid scintillator detector under construction in Jiangmen, China, whose goal is to determine the neutrino mass hierarchy.

Its data taking is expected to start in 2022. In order to meet the stringent requirements on the radiopurity of the liquid scintillator, the OSIRIS pre-detector is being designed to monitor the liquid scintillator during the several months of filling the large volume of JUNO. OSIRIS will contain 20 ton of scintillator and will be equipped with 76 20-inch PMTs. The data acquisition system will have no global hardware trigger: instead, each PMT will provide a data-stream composed of the digitized PMT pulses, each containing a time stamp. Based on the latter, dedicated software will organize these data streams into events. This talk will discuss the optimization of the event trigger conditions, for the inner liquid scintillator detector as well as outer water Cherenkov detector, considering the expected rates of different radio-active contaminations, cosmogenic muons, and the PMT dark rates.

T 20.8 Mon 17:45 Tt

Development towards an active Muon Veto System for the IAXO Experiment — •Shivani Shivani, Elisa Ruiz Chóliz, and Matthias Schott — Johannes Gutenberg-University Mainz

A ray tracing code has been developed to simulate photons generated by muons passing through scintillator coupled with SiPMs. The code models the rectangular geometry of detector and optical properties of the scintillator. This work concentrates on simulating photon transportation in a scintillator detector. A preliminary study comparing the experimental and stimulated efficiencies of the detector are presented.

T 20.9 Mon 18:00 Tt

Optimizations and Upgrades to the SuperCDMS SNOLAB L1 Trigger System — •Hanno Meyer zu Theenhausen, Lea Burmeister, Fatema Thasrawala, Matthew Wilson, Alexander Zaytsev, and Belina von Krosigk — Universität Hamburg

The SuperCDMS SNOLAB dark matter search experiment targets sensitivity toward nuclear- and electron-recoil interactions with deposited energies as low as a few eV. This puts requirements on the resolution, efficiency, noise rejection, and throughput capacity of the employed trigger system. To accomplish this, the SuperCDMS trigger system is implemented on an FPGA on custom-hardware detector readout cards. Using a multi-modular architecture, input waveforms from the detector channels are downsampled, filtered, and subjected to a flexible threshold- and trigger logic. The filtering step is achieved via an FIR filter of which the coefficients resemble a time-domain optimal filter. This presentation gives an overview about the trigger system and reports on parameter optimizations regarding the downsampling and FIR filtering modules. Finally an outlook is given on a near future upgrade involving noise correlations between individual input channels, as well as a far future upgrade about triggering using an FPGA-level neural network.