T 41: DAQ, trigger and electronics II

Time: Tuesday 16:00–18:00 Location: Tp

T 41.1 Tue 16:00 Tp

Particle Track Fitting in Hardware for the ATLAS Phase II Update — •Joachim Zinsser, Sebastian Dittmeier, and André Schöning — Physikalisches Institut, Universität Heidelberg, Deutschland

Due to the planned increase in luminosity during the ATLAS Phase II Upgrade, it is necessary to filter interesting events more efficiently. It is planned to install a filter based on the particle tracks, which, have to be evaluated in real time. The parameters of the helix-shaped trajectories can be approximated linearly.

This task is well suited for an implementation in hardware since, on the one hand, it requires only basic arithmetics and comparisons, and, on the other hand, it can be implemented in a highly parallel hardware architecture, e.g. by exploiting FPGAs.

The *Hardware Track Trigger* (HTT) group of ATLAS-TDAQ decided to follow an approach that utilizes a database of simulated trajectories. The Track-Fitter is implemented on the *Intel Stratix 10* with an integrated *High Bandwidth Memory* (HBM) for storing the constants for the linear fit of the parameters. The FPGA will be mounted on a mezzanine board that connects it to a group of *Associate Memory ASICs* that store the simulated trajectories.

This talk will focus on the way in which the fit parameters are calculated within the FPGA-logic.

T 41.2 Tue 16:15 Tp

Towards SLDO characterisation in ITkPixV1 — •Charlotte Perry, Florian Hinterkeuser, Matthias Hamer, Hans Krüger, Fabian Hügging, and Klaus Desch — Physikalisches Institut der Universität Bonn

At the high luminosity upgrade of the LHC at CERN the ATLAS Inner Detector (ID) will be replaced by an all-silicon inner tracker (ITk) consisting of an inner pixel and an outer strip detector. Compared to the current pixel detector, the upgrade will cover a significantly larger phase space while featuring a smaller pixel size.

In order to optimise the material budget, considering the increased current consumption per chip and the significantly higher number of readout chips in the upgraded pixel detector, a serial power scheme of modules had been chosen. In this scheme, a chain of modules is connected in series and supplied with a constant current. The readout chip supply voltage is generated from this constant current by on-chip Shunt-LDO (SLDO) regulators.

The SLDO is an integral part of this kind of powering scheme. It has been extensively tested with several generations of test chips, advancing its design towards the implementation in the first full size readout chip for the upgraded ATLAS pixel detector, the ITkPixV1 readout chip. In this presentation, a first characterisation of the SLDO in the ITkPixV1 is given.

T 41.3 Tue 16:30 Tp

Scan Automated Testing for the ATLAS Pixel Detector — Marcello Bindi[1], Tobias Bisanz[2], Arnulf Quadt[1], and •Christian Scheulen[1] — [1]II. Physikalisches Institut, Georg-August Universität Göttingen — [2]CERN, Geneva, Switzerland

The ATLAS Pixel detector data acquisition system (DAQ) is distributed over several different physical components, such as front-end detector modules, read-out drivers, and PCs for operating and calibrating the detector. As a result, time-consuming manual tests are currently required to ensure the correct operation of the entire system after software or firmware changes in any component.

To simplify software validation and free up manpower, a suite of automated tests is being developed for deployment in the DAQ software's continuous integration system on GitLab. Fully automated testing is only possible without involvement of the detector modules, whose operation requires some degree of manual supervision. Therefore, emulated detector responses are used for tests of readout-chain components under exclusion of the detector modules themselves.

This talk will present the initial stages of scan automated testing development, consisting of the fundamental test infrastructure and the first emulated scan tests for software validation.

T 41.4 Tue 16:45 Tp

b-jet triggers in ATLAS Run-3 — •Christian Nass[1], Tatjana Lenz[1], Jochen Dingfelder[1], and Carlo Schiavi[2] — [1]Physikalisches Institut, Universität Bonn, Germany — [2]Dipartimento di Fisica, Università di Genova, Genova, Italy

In high energy particle physics b-quarks play an important role for numerous reasons, e.g. 3rd generation particle, long lifetime, large couplings to top-quark and Higgs Boson. The latter point is crucial for many top-quark and Higgs analyses. Some of these analysis like $HH \to bbbb$, ttH or $bH \to bbb$ have fully hadronic final states. The challenge is to select these events out of the overwhelming QCD background. Since not all events can be recorded, this has to be done in real-time. Therefore a lot of effort has been put in developing algorithms to discriminate b-quark initiated jets from c-quark, light-quark and gluon initiated jets by utilising the b-quark properties. These algorithms form the b-jet triggers and have to be fast and efficient in order to keep the p_{T}-threshold as low as possible.

This talk will present the b-jet trigger code structure for ATLAS in Run-3 as well as its validation.

T 41.5 Tue 17:00 Tp

Jet algorithm performance studies of the Phase-1 upgrade of the ATLAS Level-1 Calorimeter Trigger — •Lisa Marie Baltes — Kirchhoff-Institute for Physics, University Heidelberg, Germany

The ATLAS Level-1 Calorimeter Trigger (L1Calo) identifies events containing objects such as electrons, photons, tau leptons, jets and missing transverse energy and therefore plays an important role in the data taking process of the ATLAS detector. In order to address the challenges introduced by the increased luminosity of the Large Hadron Collider in Run 3, the L1Calo Phase-1 upgrade includes several hardware and software-based updates. Within the new system, the granularity of the data from the electromagnetic calorimeter being sent to the L1Calo trigger is increased by a factor of 10. Instead of using trigger tower information, the trigger readout in Run 3 consists of so-called supercells. Several new trigger algorithms, which are implemented via FPGAs, are developed to maintain a good trigger performance even in high pile-up conditions. In order to evaluate the rates of these Run 3 algorithms, Run 2 data is used by merging the offline cells into Run 3 supercells. This can be cross-checked using Monte Carlo simulations. This talk motivates the use of the supercell emulation and shows preliminary results of the jet algorithm performance studies.

T 41.6 Tue 17:15 Tp

A FPC for the ATLAS High Granularity Timing Detector Demonstrator — •Marisol Robles Manzano[1], Peter Bernhard[2], Andrea Brogna[2], Atila Kurt[2], Karl-Heinz Geib[1], Lucia Masetti[1], Binh Pham[2], and Quirin Weitzel[2] — [1]Institut für Physik, Johannes-Gütenberg Universität Mainz — [2]PRISMA$^+$ Detector Lab, Johannes-Gütenberg Universität Mainz

The ATLAS detector requires upgrades to exploit the physics potential of new HL-LHC, where the large increase of pile-up interactions is a main challenge. The High-Granularity Timing Detector (HGTD) will be built in order to mitigate the effects of pile-up in the ATLAS forward region, providing a time resolution of about 30 ps per track. A 2x4 cm^2 Low Gain Avalanche Detector (LGAD sensor) bump-bonded to two ASICs and glued to a flexible PCB, make up the so-called module, the HGTD basic unit. The active area consists of 2-doubled-sided disks per end-cap and is surrounded by the Peripheral Electronics Boards (PEB). A Flexible Printed Circuit (Flex tail) serves as connection between a module and the PEB: power, communication signals and HV bias. A demonstrator is proposed to test the functionality and assembly of a subset of components of the full detector such as electronics, sensors and the cooling system as part of the R&D phase. A Flex tail prototype is planned to be tested during the demonstrator activities. An overall description of the demonstrator activities with emphasis on the Flex tail is presented.

T 41.7 Tue 17:30 Tp

Development of a DC-DC converter for powering the Mu3e detector — •Sophie Gagneur for the Mu3e-Collaboration — Institute of Nuclear Physics, Johannes Gutenberg University Mainz

The Mu3e experiment under construction at the Paul Scherrer Institute, Switzerland, aims to search for the lepton flavour violating decay

of a muon into one electron and two positrons with an ultimate sensitivity of one in 1016 muon decays.

The detector for the Mu3e experiment consists of High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) combined with scintillating tiles and fibres. The detector ASICs need a supply voltage of around 2V. This voltage is generated from the 20V external supply via switching DC-DC converters. These buck converters must be able to operate within a magnetic field and provide a constant output voltage with a ripple of less than 10mV to guarantee a proper operation of the pixel sensors and timing detectors. A first version of the converter has been successfully tested in the laboratory and with a prototype pixel sensor. The second version of the Mu3e DC-DC converter has been designed and produced based on the findings from these tests. The innovations in the design of these converters include an improved output filter, a temperature interlock and a current sense measurement.

T 41.8 Tue 17:45 Tp

Large Area Avlanache Photodiode gain optimization — •Kim Tabea Giebenhain — Justus-Liebig-Universität, Gießen, Deutschland

The PANDA EMC, a calorimeter with high energy resolution, is an extremely important factor in reconstruction and particle identification, especially in the lower energy range. Its PWO-II crystals are read out with two Large Area Avalanche Photodiodes. Since the energy resolution and the noise of the LAAPDs depend on the bias voltage a study was done to find the optimal bias voltage in a range between 10 MeV and 2 GeV, using a single LAAPD and the APFEL ASIC preamplifiers. In order to simulate signals a LED-Pulser, planned for an online monitoring system, was used. Those light-pulser measurements indicate, that especially for energies below 1 GeV the energy resolution can be vastly improved by using much higher amplification than a standart gain of 150.