T 66: DAQ, trigger and electronics III

Time: Wednesday 16:00–18:15 Location: Tp

T 66.1 Wed 16:00 Tp

Power Distribution in the Mu3e Experiment — •Lucas Sebastian Binn for the Mu3e-Collaboration — PRISMA+ Cluster of Excellence and Institute of Nuclear Physics, Johannes Gutenberg University Mainz

The Mu3e experiment at PSI searches for new physics utilizing the lepton-flavor-violating decay of a positive muon into two positrons and one electron. The detector consists of a lightweight tracker built from high-voltage monolithic active pixel sensors complemented by scintillating tiles and fibres for precise timing measurements. Powering of the pixel sensors and scintillating detector poses unique challenges, requiring voltages in the range of 2.0V to 3.3V and currents of up to 21A per power partition. The experiment will supply these by using DC-DC converters placed as close as possible to the consumers inside the detector's magnet. The converters step-down 20V, produced by external commercial power supplies, to the required voltages. In the final experiment, 16 converters will be mounted together in one crate. A first prototype crate has been designed and produced, providing space for four board and using an external controller. To allow high-current operation, a custom water-cooling solution has been designed and is currently being tested.

T 66.2 Wed 16:15 Tp

Firmware and Synchronisation of the First Layer in the Mu3e DAQ System — •Martin Müller for the Mu3e-Collaboration — Institute for Nuclear Physics, JGU Mainz

The Mu3e experiment will search for the lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ and is aiming for a sensitivity of one in 10^{16} muon decays. Since this decay is highly suppressed in the Standard Model to a branching ratio of below $\mathcal{O}(10^{-54})$, an observation would be a clear sign for new physics.

In the Mu3e detector, four layers of silicon pixel sensors will be used to track electrons and positrons and a time resolution of $\mathcal{O}(100$ ps) will be provided by scintillating tile and fibre detectors. The overall detector is expected to produce a data rate from 80 Gbit/s (Phase I) to 1 Tbit/s (Phase II), which will be processed in a three-layer, triggerless DAQ system using FPGAs and a GPU filter farm for online event selection.

The first layer of the DAQ system consists of 114 FPGA boards inside the 1T solenoid magnet responsible for configuration, data readout and synchronisation of the three detector types. The talk will discuss the firmware for these boards and the implementation of the clock and reset distribution in the Mu3e DAQ system.

T 66.3 Wed 16:30 Tp

Hit synchronisation in the Mu3e DAQ — •Marius Köppel for the Mu3e-Collaboration — PRISMA+ Cluster of Excellence and Institute of Nuclear Physics, Johannes Gutenberg University, Mainz Germany

The Mu3e experiment at the Paul Scherrer Institute searches for the decay $\mu^+ \to e^+e^+e^-$. This decay violates lepton flavour conservation - any observation would be a clear indication for Physics Beyond the Standard Model. The Mu3e experiment aims for an ultimate sensitivity of one in 10^{16} μ decays. To this end, more than one billion μ tracks per second need to be detected and reconstructed.

Since the corresponding data of about 1TB/s cannot be saved to disk, a trigger-less online readout system is required which is able to sort, align and analyze the data while running. A farm with PCs equipped with powerful graphics processing units (GPUs) will perform the data reduction. The talk presents the ongoing integration of the sub detectors into the Field Programmable Gate Array (FPGA) based readout system and the hit synchronisation between different parts of the detector.

T 66.4 Wed 16:45 Tp

Tile Rear Extension (TREX) Modul — •Damir Rassloff and Tigran Mkrtchyan — Kirchhoff-Institut für Physik, Heidelberg

During the phase-I upgrade of the ATLAS experiment, the Level-1 Calorimeter (L1Calo) trigger system is also undergoing a series of improvements. For the identification of isolated particles and jets the upgraded L1Calo trigger system is using new subsystems so called feature extractors (FEXes). The FEXes directly receive digitized data from the LAr Calorimeter. The Tile Calorimeter, on the other hand still send analog data to the L1Calo PreProcessor subsystem. In order to provide digitized hadronic transverse energy results at the LHC clock frequency from the Tile Calorimeter to the FEXes, the PreProcessor is being extended with new Tile Rear Extension (TREX) modules. The modules send the data to the FEX processors via optical fibers operating at 11.2 Gbps, while also maintaining the data path to the legacy L1Calo processors via electrical cables. This talk discusses the design, the different data paths and the monitoring of the TREX modules.

T 66.5 Wed 17:00 Tp

Entwicklung von algorithmischer Firmware für den Ausbau des ATLAS Level-1 Jet/Energiesummen-Triggers — Volker Büscher, Ralf Gugel, Christian Kahra, Ulrich Schäfer, Stefan Tapprogge und •Marcel Weirich — Johannes Gutenberg-Universität Mainz

In den kommenden Ausbaustufen des LHC werden immer höhere Luminositäten erreicht. Dadurch werden auch immer größere Herausforderungen an das Triggersystem des ATLAS Detektors gestellt. Zusätzlich zu den steigenden Ereignisraten werden die Daten aus den elektromagnetischen und hadronischen Kalorimetern mit erhöhter Granularität übertragen. Um dies für eine effiziente Selektion von Ereignissen zu nutzen, muss das existierende System ausgebaut werden. Bei einer Datenrate von 40 MHz muss in der ersten Triggerstufe eine Entscheidung innerhalb von 2.5 μs getroffen werden.

Der jet Feature EXtractor, kurz jFEX, bildet eine Neuerung für den Ausbau des ATLAS Level-1 Triggers. Ab 2022 wird jFEX in erster Linie für die Identifikation von Jet-Kandidaten und zur Berechnung von Energiesummen eingesetzt. Pro Modul ist eine Eingangsbreite von bis zu 2.7 Tb/s erforderlich, die sich auf 4 Xilinx UltraScale+ FPGAs verteilt. Für die dort laufenden Algorithmen stehen maximal 125 ns an Berechnungszeit zur Verfügung. Aus diesem Grund müssen diese eine hochparallele Struktur aufweisen.

In diesem Vortrag wird der aktuelle Stand der Algorithmen-Implementierung vorgestellt.

T 66.6 Wed 17:15 Tp

Demonstrator for ATLAS LAr Phase-II readout chain — •Markus Helbig, Rainer Hentges, and Arno Straessner — Institut für Kern- und Teilchenphysik, TU Dresden, Germany

A demonstrator for the readout chain of the Phase-II upgrade of the ATLAS Liquid Argon Calorimeters is being set up at the TU Dresden. This talk will give an overview of the source part of the setup representing the transmission of data from the detector Front-End Boards to the counting room.

For this purpose, dedicated VHDL firmware for the Xilinx VC707 FPGA Evaluation Kit was implemented to emulate the output of twelve on-detector ADCs of the calorimeters. The raw data are serialized by the lpGBT ASIC (Low Power GigaBit Transceiver) designed by CERN and transmitted to the off-detector backend via optical fiber at 10 Gigabit per second using the CERN Versatile Link PLUS (VL+) module. The two aforementioned components are part of a custom PCB, developed by B. Deng et al. [1] who previously showed the suitability of those components for the ATLAS LAr calorimeter readout. Finally, the backend consists of an Intel Stratix-10 FPGA development kit running parts of the Liquid Argon Signal Processor (LASP) firmware in order to receive and decode the data. Results from data integrity tests and experience with the setup will be presented.

[1] B. Deng et al., Design and hardware evaluation of the optical-link system for the ATLAS Liquid Argon Calorimeter Phase-II Upgrade, Nucl. Instrum. Methods Phys. Res., A 981 (2020) 164495

T 66.7 Wed 17:30 Tp

First level EM trigger algorithms in the ATLAS forward region for the HL-LHC — •Julian Fischer and Stefan Tapprogge — Institut für Physik, Johannes Gutenberg-Universtät, Mainz

The High-Luminosity Large Hadron Collider (HL-LHC) at CERN is a planned upgrade of the Large Hadron Collider (LHC) that will increase its instantaneous luminosity of up to a factor of five in pp-collisions. In order to exploit the full potential of the HL-LHC the first level trigger of the ATLAS experiment will have to efficiently find electromagnetic objects in the forward region, corresponding to pseudorapidity ranges

of $|\eta| > 2.5$. A dedicated 'forward Feature EXtractor' (fFEX) is in development for the high-luminosity upgrade to trigger jets as well as electromagnetic objects in the ATLAS forward region making use of the full granularity of the calorimeters. Dedicated hardware modules with FPGAs are to be developed to cover both forward directions of the detector in order to process the large amount of data delivered by the HL-LHC. This contribution will highlight the development of candidate algorithms that are designed to trigger electromagnetic objects on the fFEX modules. Performance studies will be shown and different concepts investigated to tackle the challenging geometries in this particular detector region while considering the restrictions imposed by the firmware implementation.

T 66.8 Wed 17:45 Tp

Development of an FPGA Implementation of Convolutional Neural Networks for Signal Processing for the Liquid-Argon Calorimeter at ATLAS — Anne-Sophie Berthold, Nick Fritzsche, Rainer Hentges, Arno Straessner, and •Johann Christoph Voigt — TU Dresden, Germany

With the planned Phase 2 upgrade of the ATLAS detector at LHC, the number of proton-proton collisions occuring at the same time will increase significantly. This leads to higher requirements for the data processing, since the rate of detected particles in one detector cell will increase. New machine learning solutions are under development to better reconstruct the energy deposited in the calorimeter and its timing information than the current optimal filter approach.

Here an implementation of convolutional neural networks for FPGA hardware is introduced. The network architecture is flexible and can be configured directly from the model files after network training. It is optimized regarding signal delay and resource usage. Especially the efficient use of the digital signal processors used for multiplications is crucial, since their availability is the limiting factor for network size. Respective performance and resource usage results are presented. The current status of the time division multiplexing, which is necessary to handle the high number of detector readout channels and process multiple input streams per network, is shown.

T 66.9 Wed 18:00 Tp

Evaluation einer netzwerkbasierten Detektorauslese unter Nutzung neuer Netzwerktechnoligien — •Carsten Dülsen, Tobias Flick, Wolfgang Wagner und Marius Wensing — Bergische Universität Wuppertal

Mit steigender Komplexität und höherem Auflösungsvermögen von kommenden Detektorsystemen wie dem ATLAS ITk Pixel Detektor steigt auch die zu übertragende Datenmenge weiter an. Während FPGA-basierte Auslesekomponenten die notwendigen Datenraten problemlos unterstützen, stellt die Schnittstelle zwischen FPGA und Auslesesoftware meist eine Engstelle dar. Für die Übertragung von Auslesedaten vom FPGA zur Auslese-Software wird ein Ansatz vorgestellt, bei dem die Daten über ein kommerzielles Netzwerk mittels Standardprotokollen versendet werden. Dazu wurde ein 100 GbE Netzwerk-Stack im FPGA umgesetzt. Um die Komplexität des FPGA-Systems zu reduzieren, soll die Übertragung ohne erneutes Versenden der Daten auskommen, damit auf eine Zwischenspeicherung verzichtet werden kann. Diese Strategie setzt eine Reduzierung des Paketverlustes auf ein Minimum voraus. Das Zusammenspiel von Hardware und Software wurde untersucht und das Übertragungssystem auf die Vermeidung von Paketverlusten optimiert. Auf der Software-Seite wird in diesem Zusammenhang eine eXpress Data Path (XDP) genannte Technik erprobt und ihre Eignung für die Reduzierung von Übertragungsverlusten untersucht.