T 14: DAQ and Trigger 1

Time: Monday 16:15–18:30 Location: T-H27

T 14.1 Mon 16:15 T-H27

A readout system for the LHCb Beam Condition Monitor based on off-the-shelf FPGA hardware — •Martin Bieker, Holger Stevens, and Dirk Wiedner — Experimentelle Physik 5, TU Dortmund

The LHCb experiment is a single-arm forward spectrometer at the LHC and focuses on measurements in the b and c quark sector. Due to its unique geometry, featuring a sensitive tracking system located as close as 3.5 mm to the LHC beams, the detector is at risk of damage from adverse beam conditions. For this reason, the particle flux is monitored near the beam pipe by 8 diamond sensors in a circular arrangement at either side of and close to the interaction point.

This so-called Beam Condition Monitor (BCM) successfully protected the LHCb detector during Run I and Run II of the LHC. In preparation for the following Run III, the BCM is overhauled as part of a comprehensive upgrade of the LHCb detector. The development of a new readout system is an important part of the BCM related improvements. This system is responsible for monitoring the BCM data and initiating a beam abort in case adverse beam conditions are detected.

This talk will give an overview of the new readout system and the accompanying firmware developments: A flexible architecture based on commercially sourced FPGA boards is presented and the integration into the existing LHCb DAQ framework is outlined.

T 14.2 Mon 16:30 T-H27

Modular and scalable Timepix3 readout system — Klaus Desch, •Markus Gruber, Tomasz Hemperek, Jochen Kaminski, and Tobias Schiffer — Physikalisches Institut, Universität Bonn, Nußallee 12, 53115 Bonn

With the highly granular pixel ASIC Timepix3 several different detectors can be built by combining it either with a bump bonded sensor, with a photolithographically postprocessed MicroMegas gas amplification stage (InGrid) or with a micro-channel plate (MCP). With these combinations quite different applications like beam telescopes, X-ray detectors for axion search and polarimetry and neutron detectors can be realised.

Based on the basil framework we are developing a Timepix3 readout system which can efficiently adapt these applications that range from single chip to multi-chip designs and from low- to high-rate applications. Furthermore we are implementing a flexible monitoring system that is needed to support a range of data sources depending on the detector. The hardware consists of our own PCB designs and a support of multiple FPGA boards including the Scalable Readout System (SRS) which offers scalability in low to medium rate multi-chip applications.

In this talk I will present the readout and control system and how it scales for the applications. Furthermore, I will show how the modular approach enables several different detector designs and offers the needed functionality like calibration, equalisation, readout and monitoring.

T 14.3 Mon 16:45 T-H27

Upgrade of a cosmic muon teststand for the CMS DT-Project — •Dmitry Eliseev, Thomas Hebbeker, Markus Merschmeyer, and Matej Repik — Physics Institute III A, RWTH Aachen University

The Drift Tube (DT) system is one of the muon detectors of the Compact Muon Solenoid (CMS). The DT system is now upgraded to provide the increased luminosity for CMS Phase II. The upgrade pertains mainly the on-chamber digital readout and the subsequent data chain, which are completely replaced to enable higher acquisition rates and better trigger flexibility. The especially important component of the data chain is the electronics for digital readout of the muon hit data. This is the newly designed On-Board Drift Tube (OBDT) electronics, located directly at the DT chambers. This electronics enables higher data acquisition rates and is radiation tolerant. After production, the OBDT electronics will require numerous verification tests. One of the verification sites will be RWTH Aachen University with its cosmic muon teststand, originally developed during CMS construction. The core part of the muon teststand is a fully functional DT chamber, which is similar to the DT chambers at CMS. For the upcoming verification tests the teststand has undergone a comprehensive upgrade. The upgrade included the complete replacement of the data system as well as the redesign and upgrade of other systems: high- and low- voltage power-supply, gas mixing system. The teststand enables in-situ tests of the newly produced OBDT electronics as well as the verification of the data integrity of the muon-data along the readout chain.

T 14.4 Mon 17:00 T-H27

Calibration of the analogue signal path of the Level-1 Calorimeter Trigger after the ATLAS Phase-I upgrade — •Thomas Junkermann — Kirchhoff-Institut für Physik, Heidelberg

The Phase-I Upgrade of the ATLAS Level-1 Calorimeter Trigger targets a finer granularity of the spatial information of energy depositions when selecting events. To process the higher amounts of data a new digital trigger is installed. Therefore new electronic components get introduced in the on-detector electronics leading up to the trigger. These components effect the old analog trigger system and re-calibration of it is needed as it will be run in Run 3 parallel to the new system. Examples for the effects of the new components on the legacy system are the introduction of time delays to certain signal parts and amplitude losses. The effects are measured and corrected for by re-adjusting the calibration of various components.

T 14.5 Mon 17:15 T-H27

Test beam studies of the new ATLAS MDT front-end electronics in the GIF++ facility at CERN — •Davide Cieri[1], Gregor Eberwein[1], Markus Fras[1], Oliver Kortner[1], Hubert Kroha[1], Chrysostomos Valderanis[2], Elena Voevodina[1], and Bastian Wesely[1] — [1]Max-Planck-Institut für Physik, Munich, Germany — [2]Ludwig-Maximilians-Universität, Munich, Germany

The front-end readout electronics of the ATLAS Monitored Drift Tube (MDT) detector will be replaced for High-Luminosity LHC operations in order to provide a triggerless read-out required by the upgraded first-level muon trigger. The read-out chain of an MDT chamber is composed of several Amplifier/Shaper/Discriminator (ASD) ASICs, capturing the arrival signal at the wires; Time-to-Digital Converter (TDC) ASICs, performing the required time measurements on 24 channels coming from three ASD ASICs, and a Chamber Service Module (CSM), which multiplexes data from up to 18 TDCs and sends the data via two optical fibres to the MDT trigger processor for the further trigger processing and transmission to the data acquisition (DAQ) system. The front-end electronics were designed to cope with a hit rate of 600 kHz/tube, which is twice the maximum expected rate.

Prototypes of the entire MDT front-end electronics were operated on MDT chambers in a muon beam at the GIF++ facility at CERN in 2021 using two small MDT chambers. The electronics were shown to work perfectly under different levels of the photon background irradiation, covering twice the range of the expected background fluxes at the HL-LHC.

T 14.6 Mon 17:30 T-H27

Scan Automated Testing for the ATLAS Pixel Detector — Marcello Bindi, Arnulf Quadt, and •Chris Scheulen — II. Physikalisches Institut, Georg-August Universität Göttingen

The ATLAS Pixel detector data acquisition system (DAQ) is distributed over several different physical components, such as front-end detector modules, read-out drivers, and PCs for operating and calibrating the detector. As a result, time-consuming manual tests are currently required to ensure the correct operation of the entire system after software or firmware changes in any component.

To simplify software validation and free up manpower, a suite of automated tests of the is being developed for deployment in the DAQ software's continuous integration system on GitLab. Fully automated testing is only possible without involvement of the detector modules, whose operation requires some degree of manual supervision. Therefore, emulated detector responses are used for tests of readout-chain components under exclusion of the detector modules themselves.

This talk will give an overview over the first version of the automated calibration testing and validation framework currently deployed for code developments on GitLab. An outlook to further developments of the testing infrastructure will be presented as well.

T 14.7 Mon 17:45 T-H27

GUI framework and configuration database for ATLAS ITk Pixel system tests — Gerhard Brandt, Marvin Geyik, •Jonas Schmeing, and Wolfgang Wagner — Bergische Universität Wuppertal

For the LHC Phase-2 upgrade, a new ITk Pixel detector will be installed in the ATLAS experiment. It will allow for even higher data rates and will be thoroughly tested in the ATLAS ITk Pixel system tests. To operate these tests, a GUI and configuration system is needed. A flexible and scalable GUI framework based on distributed microservices is introduced. Each microservice consists of a frontend GUI, a Python app served by a WSGI server, and a system-level backend. The frontend GUI is a single-page application built with the React JavaScript library. It uses PatternFly, which provides many UI elements as React components. The API for RESTful HTTP communication between the frontend and the Python app is defined via an OpenAPI specification. The Python app is the central part of each microservice. It connects to the microservices backend, such as a database or various DAQ applications that provide a Python binding. With this microservice framework, it is possible to serve specialized applications for different purposes: e.g., an API to access the data acquisition software, a service for configuration of hardware components, and a database to store these configurations. To enable users to access all services from a single web page, all frontend GUIs are compiled into one chassis. The REST and Python interfaces facilitate the maintainability and long-term upgradability of the system.

T 14.8 Mon 18:00 T-H27

The First Layer of the Mu3e Data Acquisition System — •Martin Müller for the Mu3e-Collaboration — Institute for Nuclear Physics, JGU Mainz

The Mu3e experiment will search for the charged lepton flavor violating decay of a positive Muon into two positrons and one electron. The branching ratio of this decay in the Standard Model is predicted to be in the order of 10^{-54} and therefore any observation of such a decay would be a clear sign for new physics. Observing up to 10^8 muon decays per second, the phase I Mu3e detector will produce 100 GB/s of data from monolithic pixel chips, scintillating fibres and scintillating tiles.

The trigger-less data acquisition for the detector consists of multiple layers. Layer 1 is located inside of the Mu3e magnet and is directly connected to the detector readout ASICs with 1.25 Gbit data links. It is built from 112 Frontend-Boards which include two field programmable gate arrays (FPGAs). These FPGAs are responsible for all communication with the different detector ASICs, including data readout, decoding, sorting, synchronisation and also the configuration of the detectors. The talk will discuss the firmware developed for the FPGAs in Layer 1 of the Mu3e DAQ and the interfaces to the other DAQ layers.

T 14.9 Mon 18:15 T-H27

Data Flow in the Mu3e Filter Farm — •Marius Köppel for the Mu3e-Collaboration — Institute for Nuclear Physics, Johannes Gutenberg University, Mainz Germany

The Mu3e experiment at the Paul Scherrer Institute searches for the decay $\mu^+ \to e^+e^+e^-$. This decay violates charged lepton flavour conservation - any observation would be a clear indication for Physics Beyond the Standard Model. The Mu3e experiment aims for an ultimate sensitivity of one in 10^{16} μ decays. The first phase of the experiment, currently under construction, will reach a branching ratio sensitivity of $2 \cdot 10^{-15}$ by observing 10^8 μ decays per second over a year of data taking. The highly granular detector based on thin high-voltage monolithic active pixel sensors (HV-MAPS) and scintillating timing detectors will produce about 100 GB/s of data at these particle rates.

Since the corresponding data cannot be saved to disk, a trigger-less online readout system is required which is able to sort, align and analyze the data while running. A farm with PCs equipped with powerful graphics processing units (GPUs) will perform the data reduction. The talk presents the ongoing integration of the sub detectors into the Field Programmable Gate Array (FPGA) based readout system, in particular focusing on the data flow inside the FPGAs of the filter farm. It will also show insides of the DAQ system used in the Mu3e Integration Run performed in Spring 2021.