T 97: Electronics 1

Time: Thursday 16:15–18:00 Location: T-H28

T 97.1 Thu 16:15 T-H28

Instrumentation of a GEM-Based Neutron Detector — •Laura Rodríguez Gómez[1], Saime Gürbüz[1], Jochen Kaminski[1], Markus Köhli[2], Michael Lupberger[1], Divya Pal[1], and Klaus Desch[1] — [1]Universität Bonn — [2]Universität Heidelberg

The VMM chip, originally developed for the ATLAS New Small Wheel Upgrade, was implemented in the multi-purpose readout system of the RD51 collaboration over the last years. Within this so-called Scalable Readout System (SRS) the frontend board is called VMM hybrid as it holds two frontend chips as well as an FPGA and other electronic components to handle data and powering. This system provides a complete readout chain for a large variety of particle detectors.

For the developement of a multilayer Gas Electron Multiplier (GEM) - based neutron detector, a larger system of hybrids is planned, set up and tested. This includes not only the high voltage protection of the readout electronics and the power stability of all hybrids, but also the design of a cooling system and a mechanical suspension.

The detector concept, VMM hybrid test results and measurements with a test layer are presented. The application of VMM hybrids and GEMs in multilayer neutron detectors as a technology transfer is discussed.

T 97.2 Thu 16:30 T-H28

Development of a DC-DC converter for powering the Mu3e detector — •Sophie Gagneur for the Mu3e-Collaboration — Institut für Kernphysik, JGU Mainz

The Mu3e experiment under construction at the Paul Scherrer Institute, Switzerland, aims to search for the lepton flavour violating decay of a muon into one electron and two positrons with an ultimate sensitivity of one in 10^{16} muon decays. The Mu3e detector consists of a tracker based on High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) combined with scintillating tile and fibre timing detectors. The detector ASICs need a supply voltage of around 2V. This voltage is generated from the 20V external supply voltage via switching DC-DC converters. These buck converters must be able to operate within a magnetic field and provide a constant output voltage with a ripple of less than 10mV to guarantee a proper operation of the pixel sensors and timing detectors. The second version of the Mu3e DC-DC converter has been designed, produced and already tested successfully in the laboratory, implementing features such as a secondary output filter and a temperature interlock for the pixel sensors. The final version is currently being designed and integrated into the experiment to be used during the upcoming commissioning runs.

T 97.3 Thu 16:45 T-H28

Powering Scheme of the Tracking Detector of the P2 Experiment at MESA — •Lars Steffen Weinstock — PRISMA+ Cluster of Excellence and Institute of Nuclear Physics, Johannes Gutenberg University Mainz

P2 is a precision experiment planned for the Mainz Energy recovering Superconducting Accelerator (MESA) currently under construction. The goal of P2 is to determine the electroweak mixing angle at low energy scales with unprecedented precision by measuring the parity violating asymmetry in proton-electron scattering at low momentum transfer. A key parameter for the analysis, the electron momentum transfer during scattering, is measured by the P2 tracker, which is placed inside the 0.6 T solenoid spectrometer. The tracker consists of eight identical modules utilising a total of 4320 novel High Voltage Monolithic Active Pixel Sensors (HV-MAPS) for precise track reconstruction. With each HV-MAPS drawing about 1W the tracker frontend requires more than 5kW of power, which is supplied to the tracker using a remote-sense technique. This talk presents the current state of the powering scheme of the P2 tracking detector, key design parameters, and technical details of the implementation including first test measurements.

T 97.4 Thu 17:00 T-H28

A Simulation Framework to Optimize Signal Processing for Particle Detectors — •Florian Rössing[1], André Zambanini[1], Christian Grewing[1], and Stefan van Waasen[1,2] — [1]ZEA-2, Forschungszentrum Jülich GmbH — [2]NTS, University of Duisburg-Essen

Particle Detectors evolve to ever higher performance, both in terms of sensitivity and channel density. This increases the amount of data to be handled. As transmitting this raw data is often not a viable option, data reduction has to be employed. To achieve this, the individual channel signals are converted, and the data is processed close to the sensor, extracting observable parameters of the signal. Recent developments often rely on low-level, analog blocks and simple digitizers as signal converters, which are tailored to the specific sensor used in the detector. This limits reusability, making a repeated design effort necessary. The design of generic readout electronics based on digital data processing could overcome this issue. In a pursuit to build such a generic detector readout, part of the necessary work is the design of a single channel signal conversion and data handling, both to be used for a wide range of detectors with different sensors. For this, MatLab and Simulink are used to study and evaluate signal and data processing chains. This includes shaping, different digitization approaches (e.g. TDC, ADC) and data processing algorithms. This contribution will describe the models used as input signals for simulations, the architecture of the simulation software, and introduce first algorithm implementations.

T 97.5 Thu 17:15 T-H28

FPC design and prototype for the ATLAS High Granularity Timing Detector Demonstrator — •Maria de la Soledad Robles Manzano[1], Peter Bernhard[2], Andrea Brogna[2], Atila Kurt[2], Karl-Heinz Geib[1], Lucia Masetti[1], Binh Pham[2], Steffen Schoenfelder[2], and Quirin Weitzel[2] — [1]Institut für Physik, Johannes-Gütenberg Universität Mainz — [2]PRISMA$^+$ Detector Lab, Johannes-Gütenberg Universität Mainz

The ATLAS detector requires upgrades to face the challenges of the new HL-LHC, mainly the increase of pile-up interactions. The High-Granularity Timing Detector (HGTD) will be built in order to mitigate the effects of pile-up in the ATLAS forward region, providing a time resolution of about 30 ps per track. The active area consists of 2-double-sided disks per end-cap. The HGTD basic unit, so-called module, is made up of two 2x2 cm^2 Low Gain Avalanche Detectors bump-bonded to two ASICs and glued to a flexible PCB. The modules are connected to the Peripheral Electronics Boards, surrounding the active area, via a Flexible Printed Circuit (Flex tail) that serves as interconnection for power, communication signals and HV bias. As part of the HGTD R&D phase, a demonstrator is proposed to test the functionality and assembly of a subset of components of the full detector. The design and tests of a Flex tail prototype in the context of an overall description of the demonstrator activities are presented.

T 97.6 Thu 17:30 T-H28

Prototyping Serial Powering with RD53A — Klaus Desch, Matthias Hamer, •Florian Hinterkeuser, Fabian Hügging, Hans Krüger, Charlotte Perry, and Lars Schall — Physikalisches Institut, Universität Bonn

The high luminosity upgrade for the Large Hadron Collider at CERN requires a complete redesign of the current inner detectors of ATLAS and CMS. These new inner detectors will consist of all-silicon tracking detectors. A serial powering scheme has been chosen as baseline for the pixel detector to cope with the higher number of modules and the higher power consumption of the new front-end chip, spatial constraints and the need to minimize the tracker's material budget. This new powering scheme provides challenges for the electrical and mechanical design. In order to verify this new powering scheme and its implications on the detector integration, efforts have been ongoing to set up a prototype for serial powering using modules based on the RD53A chip, a half-size prototype for the new Pixel front-end chip, developed by the RD53 collaboration. In particular, a serial powering stave consisting of up to 8 RD53A quad chip modules has been set up in Bonn. The results from the activities with RD53A chips are presented. Emphasis is put on the electrical characterization of an RD53A serial powering chain, using representative services and power supplies. The setup, measurement goals and characterization of the serial powering chain will be discussed.

T 97.7 Thu 17:45 T-H28

Test Results of the New ASD Chips for Phase-II Upgrade of the ATLAS MDT Chambers at HL-LHC — •Katrin

Penski, Otmar Biebel, Stefanie Götz, Vitaliy Havrylenko, Ralf Hertenberger, Christoph Jagfeld, Maximilian Rinnagel, Chrysostomos Valderanis, and Fabian Vogel — LMU München

The Phase-II Upgrade of the ATLAS Muon Spectrometer to the High Luminosity LHC (HL-LHC) requires an efficient trigger and readout system for the Monitored Drift Tube (MDT) chambers. For this purpose, new front-end electronics have been developed including an 8-channel amplifier shaper discriminator (ASD) chip built in 130 nm GF CMOS technology. Using pre-production chips, this presentation discusses the overall performance of these chips as well as the dependence on programmable parameters. Moreover, the uniformity between pre-production chips and the first batch of production chips is shown. These test results are used to define the acceptance criteria for the series testing which is planned for winter 2021. For this series testing a new tester is necessary. Its behavior is studied by retesting all chips with this tester and comparing the corresponding results with those of the previous tester.