T 49: Electronics, Trigger, DAQ II

Time: Wednesday 16:15–18:15 Location: KH 00.023

T 49.1 Wed 16:15 KH 00.023

Readout Electronics for the ECHo-LE Experiment — •Timo Muscheid, Robert Gartmann, Daniel Crovo, Matthias Balzer, and Luis Ardila-Perez for the ECHo-Collaboration — Karlsruhe Institute of Technology, Karlsruhe, Germany

Precise knowledge of the neutrino mass is crucial for solving fundamental questions in the Standard Model of Particle Physics. The ECHo collaboration aims to further limit the electron neutrino mass by analyzing the electron-capture spectrum of Holmium-163. ECHo-100k employs 10,000 detectors with a total activity of 100 kBq to improve energy resolution through increased measurement statistics. For operation of these microwave-SQUID-multiplexed pixels a custom Software-defined radio (SDR) system has been developed. This system is responsible for stimulating the resonators in the 4-8 GHz band, frequency demultiplexing and flux-ramp demodulation of the carrier tones as well as online data rate reduction. The next phase, ECHo-LE, will further increase the pixel count to 20,000 across 25 cryogenic readout lines. The room-temperature readout system will be based on the existing SDR electronics from ECHo-100k, completed by 10 additional modules. Firmware development will continue, focusing on enhanced capabilities such as tone-tracking, which promises to reduce distortion and intermodulation. In this contribution, we will present the proposed hardware architecture and firmware concept of the ECHo-LE room-temperature readout electronics. We discuss potential hardware upgrades and new firmware features of the SDR, highlighting their importance for meeting the high demands of the experiment.

T 49.2 Wed 16:30 KH 00.023

Compact and fast ADCs for pixel detectors — •Kennedy Caisley, Hans Krüger, and Jochen Dingfelder — University of Bonn, Germany

This work investigates improving analog to digital converters (ADCs) in the context of CMOS pixel detectors; a discipline with perhaps the most stringent silicon area constraints. We assembled a custom flow built on open source chip design tools, which enabled comparisons between circuit topologies and process nodes including 180, 65, and 28 nm. We then fabricated a prototype ASIC in 65 nm using this methodology, aiming for a state-of-the-art 2500 μm^2 area and 100 μW power budget, while sustaining a performance of 12-bit resolution at 10 Ms/s. Initial validation of this prototype and our on-going developments will be presented.

T 49.3 Wed 16:45 KH 00.023

Readout Electronics for the IceCube Surface Array Enhancement — •Frederik Schmitt[1], Megha Venugopal[1], Andreas Weindl[1], Alexander Novikov[2], Frank Schröder[1,2], Andreas Haungs[1], and Matthias Kleifges[3] for the IceCube-Collaboration — [1]Institute of Astroparticle Physics (IAP), Karlsruhe Institute of Technology, Germany — [2]University of Delaware, Newark, USA — [3]Institute for Data Processing and Electronics (IPE), Karlsruhe Institute of Technology, Germany

The IceCube Neutrino Observatory consists of a cubic-kilometer in-ice neutrino detector and the IceTop surface detector. IceTop comprises 81 pairs of ice-Cherenkov tanks for air-shower detection. As part of the upgrades, IceTop will be equipped with new surface stations, each consisting of eight scintillator panels and three radio antennas. Three of these stations are already in operation at the South Pole, and more are to be installed in the coming years in the area of the current IceCube experiment. The design is also the baseline for the surface instrumentation of IceCube-Gen2.

In this contribution, we focus on improvements to the current readout electronics deployed in prototype stations at IceCube, Pierre Auger, and the Telescope Array. Additionally, we present the development status of a new generation of the electronics capable of being implemented in the future IceCube and IceCube-Gen2 readout system. This design is based on a multi-FPGA board and provides GSa/s radio readout capabilities along with extensive onboard memory for signal buffering.

T 49.4 Wed 17:00 KH 00.023

Upgrade of the KlauS6 ASIC — •Yung-Wei Chang — Im Neuenheimer Feld 227, 69120 Heidelberg

In this talk, we share recent work on the KLauS ASIC, which was designed for the prototype of CALICE collaboration's Analog Hadron CALorimeter (AHCAL) and now is undergoing significant enhancements to its digital blocks and IOs to better meet the needs of future experimental applications in particle physics. The next generation of the KlauS6 ASIC will emphasize improvements in its digital interface robustness, aim at achieving higher measurement data rate and increased adaptability in experimental settings. As in previous versions, the new design incorporates strategies for low power consumption with the requirements of high-density channel applications, ensuring that the KLauS ASIC remains a cutting-edge solution for scintillator-based calorimetry in future collider experiments.

Key features of the upgraded KlauS6c include dual-configurable interfaces via both I2C and SPI, which will facilitate integration with various systems and enhance operational flexibility. Furthermore, the ASIC will support numerous speed options of LVDS readout exceeding 160 Mbps, ensuring rapid data transmission to accommodate the demands of future circular collider (FCC) experiments. Improved packaging options, compatible with QFN84 and QFN100, will provide greater reliability and ease of integration. The upgraded KlauS6c will maintain its core functionalities still on high precision charge measurement and a wide dynamic range, allowing for comprehensive and precise silicon photomultiplier (SiPM) readout behavior.

T 49.5 Wed 17:15 KH 00.023

Validation of the SiPM-on-Tile Readout Chain for the CMS High Granularity Calorimeter — •Fabian Hummer — Institute for Data Processing and Electronics, Karlsruhe Institute of Technology, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany

For the upcoming high-luminosity LHC, the endcap calorimeters of the CMS experiment will be replaced by the high-granularity calorimeter (HGCAL), a sampling calorimeter using silicon sensors in the front and plastic scintillators read out by SiPMs in the back. We have built and tested a complete horizontal slice of scintillator tile modules and readout electronics under realistic installation, grounding and powering conditions. Using this system, we validated the powering scheme, assessed the system stability and demonstrated data readout with the Serenity back-end hardware. The successful validation of the SiPM-on-Tile front-end as a complete system is an important milestone towards the construction and operation of HGCAL. In this contribution, we will describe our system validation setup and showcase results from bench-top tests.

T 49.6 Wed 17:30 KH 00.023

Enabling lpGBT Interface Prototyping with a New FPGA Mezzanine Card — •Dmitry Eliseev, Nils Esper, Carsten Presser, Markus Merschmeyer, Alexander Schmidt, and Thomas Hebbeker — III. Physikalisches Institut A, RWTH Aachen University

The lpGBT (Low Power GigaBit Transceiver) is a radiation-tolerant ASIC developed to provide robust, high-speed, bidirectional optical links for the next generation of high-energy physics experiments. It is dedicated to communicate via optical links and supports transfer rates up to 10 Gb/s. The chip integrates Timing and Trigger Control (TTC), Data Acquisition (DAQ), and Slow Control (SC) data streams into a single constant-latency link. This unified architecture enables reliable transmission of timing, trigger, control, and monitoring information between the counting room and on-detector electronics, even in the harsh radiation environment of the LHC.

This talk introduces a newly developed FMC mezzanine board that provides an accessible and flexible platform for working with the lpGBT ASIC. It gives engineers and researchers a practical way to explore, test, and integrate the lpGBT into their detector readout and control systems. With the ready to use electrical and firmware interfaces, the board supports early development without requiring a full custom electronic and firmware design.

The talk gives an overview of the board's design features, from the optical SFP link to the on-board switches for selecting lpGBT working modes. It also presents a brief overview of the IP cores for interfacing.

T 49.7 Wed 17:45 KH 00.023

ITkPix Read-out Chip Software Emulator for the ITk Pixel

Online DAQ Software — Matthias Drescher, Jörn Grosse-Knetter, •Timo Pospiech, Arnulf Quadt, and Ali Skaf — II. Physikalisches Institut, Georg-August-Universität Göttingen

During the approaching ATLAS HL-LHC phase 2 upgrade, the current Inner Detector will be replaced by the all-silicon Inner Tracker (ITk). In particular, the ITk pixel part will be composed of around 9k detector modules built with about 30k ITkPix read-out chips. The data acquisition (DAQ) read-out system needs to deal with the tremendous challenges it faces and, of course, be validated before the commissioning of the new ITk. With the read-out software as the head of the chain, it needs to be running reliably to acquire data and test other components of the DAQ chain, ideally at a large-scale system level.

To help with the development and debugging of the read-out software, a software model of the on-detector hardware is needed. As such, this project focuses on developing a standalone C++ software emulator of the ITkPix front-end, which can be used for that purpose. The software emulator faithfully replicates the behaviour of the ITkPix-V2 chip, which is the final production read-out chip. With that, the behaviour of the emulator is as close to the real conditions as possible. The emulator is validated against already existing read-out chain tools and will be integrated in the online DAQ software, allowing system-level development and debugging, but could also be used during actual data taking for validation purposes.

T 49.8 Wed 18:00 KH 00.023

Front-End Readout for the LHCb Migthy SciFi Tracker — Carlos Garcia Argos, Marco Gersabeck, •Michael Lupberger, Santiago Ochoa, Ksenia Solovieva, and Jan Sorokovski — Albert-Ludwigs-Universität Freiburg, Freiburg im Breisgau, Germany

During CERN's Long Shutdown 4, several sub-detectors of the LHCb experiment will be replaced. This upgrade is required to cope with the further increase in instantaneous luminosity and with the radiation that will accumulate until the end of the experiment's lifetime.

One of these is the tracker located downstream of the spectrometer magnet. The current tracking detector is based on Scintillating Fibres (SciFi). It will be replaced by a hybrid detector, called Mighty Tracker, that combines HV-CMOS MAPS in the central region near the beam pipe and new SciFi modules in the outer part. The latter will be read out using Silicon Photomultipliers operated at cryogenic temperatures. Their signals will be processed by a front-end chip, which is controlled and read out by lpGBT chips. The readout board is housed in a metal box that serves cooling and shielding.

This contribution presents the current status of the front-end read-out. It focuses on the key requirements and on how the design aims to satisfy them.